

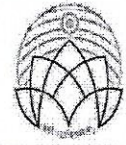
SHRI MADHWA VADIRAJA INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(A Unit of Shri Sode Vadiraja Mutt Education Trust®, Udupi)

Accredited by NAAC with 'A' grade | Affiliated to VTU, Belagavi

Approved by AICTE, New Delhi & Recognized by Govt. of Karnataka

Vishwothama Nagar, Bantakal - 574115, Udupi District, Karnataka.

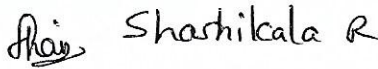
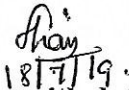

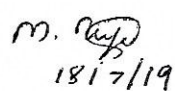



SMVITM

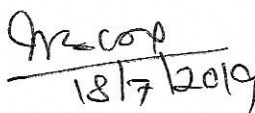

Activity Request form

| | | | |
|---------------------------------------|--|------|----------------|
| Academic Year | 2019-2020 | | |
| Department/Section/ Committee/Cell | Department of Electronics & Communication Engineering / ISTE | | |
| Name of the Activity | FDPon VLSI Chip Design and Verification using Mentor Graphics EDATool | | |
| Target Audience | Faculty members of ECE department | | |
| Activity Date(s) | 22-23 July 2019 | Time | 9:30am-4:30 pm |
| Venue | VLSILab, Dept. of ECE | | |
| Resource Person | Mr. Vijendra V. Application Engineer, CoreEL Technologies | | |

| | |
|---|----|
| Financial support required from the Institute | NO |
|---|----|

| | |
|---|---|
|  Name of the Coordinator |  Signature with date 18/7/19 |
|  Signature of the HoD (If applicable) |  Signature of the ISTE Coordinator 18/7/19 |

| | |
|---|--|
| <u>Remarks by IQAC</u> | |
| May be conducted | |
|  Signature 18/7/19 | |

| | |
|--|--|
| <u>Remarks by Principal</u> | |
| Very good step. Proceed | |
|  18/7/2019 | |
|  Signature | |

Principal
SHRI MADHWA VADIRAJA
INSTITUTE OF TECHNOLOGY & MANAGEMENT
Vishwothama Nagar, Udupi Dist.
BANTAKAL - 574 115

Instructions

Coordinators are requested to get the approval from the Principal at least one week before the activity.

Name of the activity:

- Invited Talk, Seminar, Workshop, Competitions
- Placement training programs to Students
- Placement drives
- FDP, EDP, Conference, staff development program
- First year Orientation day, Annual Day, Varnotsava, Graduation day, Sports day, games competitions, Avishkar, IIOT, Project Exhibition, Farewell Program
- Inauguration/Valedictory of Cell/Clubs
- Alumni meet, PTA meet
- College promotional activity, career guidance program

Target Audience (with expected number of participants):

Staff- Teaching or Non-teaching/ department

Students - Only registered students/compulsory

- Student details with class and departments

Resource Person: Name, Designation, Address and contact Number.


Expected expenditure: Includes Honorarium to resource person, TA/DA, Certificates, Food, Banner, Prize money etc.

For the department activity, coordinators are requested to get the approval from the concerned department Heads, and then submit it to IQAC.

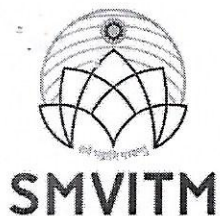
IQAC in turn verify the committee perspective plan, activities of the other committees to avoid overlapping of the activities, gives the remarks accordingly and forward the form to the Principal for the approval.

After approval from the Principal, activity shall be conducted.

Activity report with good quality photographs should be sent to the concerned within 2 days of the activity.


Principal

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Website : www.sode-edu.in

Vishwothama Nagar, Bantakal – 574 115, Udupi, Karnataka, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

ACTIVITY REPORT

| | |
|---------------------|--|
| Academic Year | 2019-20 |
| Name of activity | FDP on VLSI Chip Design and Verification using Mentor Graphics EDA Tool |
| Resource Person | Mr. Vijendra V. Application Engineer, CoreEL Technologies |
| Date | 22-23 July 2019 |
| Time | 9:30 am – 4:30 pm |
| Venue | VLSI Lab, Dept. of ECE |
| Target Audience | Faculty members of ECE department |
| No. of participants | 20 |

The department of Electronics & Communication Engineering of SMVITM Bantakal, in association with CoreEL Technologies Bengaluru and ISTE Faculty Chapter, organized a 2-day workshop for faculty members on the topic “VLSI Chip Design and Verification using Mentor Graphics EDA tool”, on 22 & 23 July 2019. Faculty members of E&C Engineering from the neighboring institutes participated in the workshop and enhanced their knowledge and skill. Mr. Vijendra V, Application Engineer from CoreEL was the resource person.

During the workshop, the participants acquired hands-on skills on the usage of latest Mentor Graphics software tools such as Questa-Sim, Leonardo, Pyxis, and Calibre, which are used in the Application Specific Integrated Circuit (ASIC) design.

Distributing the certificates to the participants, Principal of SMVITM Dr. Thirumaleshwara Bhat said that learning, re-learning and acquiring skills in latest topics should become a lifelong habit of all the faculty members. He congratulated and thanked all the external and internal participants of the workshop. Convener Dr. Balachandra Achar, coordinators Mr. Chetan R and Ms. Sowmya Bhat were present on the occasion.


Principal

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BANTAKAL - 574 115



Latitude: 13.254430
Longitude:74.785653



Latitude: 13.254776
Longitude:74.785564

Anand
Principal
SHRI MADHWA VADIRAJA
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REGISTRATION FORM

2-day FDP on

VLSI Chip Design and Verification using
Mentor Graphics EDA Tool

Name:

Designation:

Department:

Name of the Institute:

Address:

Email:

Mobile:

Bank Transaction No.

Date:

Bank Name:

Signature

Dr./Mr./Ms.
is Faculty / Student of our institute and is hereby
permitted to attend the workshop at SMVITM
Bantakal, Udupi.

Place:

Date:

Signature of Head of the
Institution / Department with Seal

Chief Patron

H. H. Shri Vishwavallabha Theertha Swamiji
President, Shri Sode Vadiraja Mutt Education Trust &
& Chairman, SMVITM Governing Council

Patrons

Shri P. Shrinivasa Tantry
Vice President, SSVMET, Udupi

Shri Rathnakumar
Secretary, SSVMET, Udupi

Chairman

Prof. Dr. Thirumaleshwara Bhat
Principal, SMVITM, Bantakal

Convener

Dr. Balachandra Achar H. V.
Professor & Head, Dept of ECE

Coordinators

Mr. Chetan R., Sr. Asst. Professor, Dept of ECE
Ms. Sowmya Bhat, Asst. Professor, Dept of ECE

Resource Persons

Mr. Vijendra V., Application Engineer
Mr. Tomin George, Sales Executive
CoreEL Technologies, Bengaluru

For Correspondence

Mob: 9481360288
Email: ec@sode-edu.in

**Two-Day
Faculty Development Program**

On

**VLSI Chip Design and
Verification using
Mentor Graphics EDA tool**

22-23 July 2019

Organized by
**Department of
Electronics & Communication
Engineering**



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AND MANAGEMENT**

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Vishwothama Nagar, Bantakal - 574115
Udupi, Karnataka

In Association with



ABOUT THE COLLEGE

Founded in 2010 by H. H. Shri Vishwavallabha Theertha Swamiji of Shri Sode Vadiraja Mutt Udupi, Shri Madhwa Vadiraja Institute of Technology & Management (SMVITM) has carved a niche for itself in imparting quality engineering education to students in coastal Karnataka region. The campus is located at Bantakal, which is about 12 km from Udupi town and 6 km from the National Highway NH-66. The college is accredited with Grade A by the National Assessment and Accreditation Council (NAAC). The management and the academic administration have been steadfast in their commitment to make SMVITM one of the best engineering institutes in South India in the very near future.



ABOUT THE DEPARTMENT

The Department of Electronics and Communication Engineering is intent on creative and technologically advanced skill transfer to students through teaching, mentoring and counseling. It regularly organizes short-term courses, seminars, symposiums, workshops, FDPs and invited talks by eminent persons from reputed institutions and industries, to keep the students and faculty members abreast of the latest technological advances in related fields.

ABOUT CoreEL TECHNOLOGIES

CoreEL Technologies (I) Pvt Ltd is a customer Application Specific Products & Solutions company offering Intellectual Property Hardware, Software & Engineering Services to customers, enabling them to Design Manufacture and Market world class electronic products. The portfolio of offerings include IP cores, System Design, Architecture, Validation, Sustenance, Prototype Manufacturing, Next-Gen products, Semiconductor solutions & Distribution of EDA Tools. Started in 1999, CoreEL is an ISO 9001:2008 certified company headquartered at Bengaluru.

ABOUT CoreEL UNIVERSITY PROGRAM

CoreEL University Program provides Eco-System support to Indian Academia in Engineering Higher Education, in the field of Embedded Systems, thereby enabling the delivery of quality education to students. CoreEL achieves this by providing state-of-the-art products from XILINX, MENTOR GRAPHICS, MATLAB, VxWorks, Speed-goat (Rapid Controller Prototyping, Hardware-in-the-Loop simulation, and deployment) PCB Design Tools from Mentor Graphics, Analog Discovery Kits from Digilent (Analog Discovery Kit can replace the conventional regulated power supply, Function Generator, Oscilloscope, and smaller parts like Breadboard etc. with one portable, compact and low cost solution!) to universities. Multiyear application engineering support on these products, Faculty and Student training, providing industry specific inputs to update the curriculum and helping universities set up Centers of Excellence in Embedded Systems arena.

TARGET AUDIENCE

Faculties from Engineering Colleges, Candidates from industries and R & D organizations, and PG Students, with Basic knowledge of HDL

REGISTRATION DETAILS

Intending participants are requested to transfer Rs. 600/- to the college account through NEFT, and send the scanned copy of duly filled Registration Form by email to ec@sode-edu.in
Bank Name: Bank of Baroda, Innanje Branch
A/C Name: SMVITM Bantakal, Current Account
A/C No. 16580200000081, IFSC: BARB0INNANJ

WORKSHOP CONTENTS

Day-1:

- Fundamentals of VLSI Chip Design Methodology
 - Basics of ASIC & FPGA
- Demonstration of HDL Design flow for front end, with hands-on
 - Simulation using Modelsim
- ASIC Semi-custom methodologies with Pyxis hands-on session
 - Area calculation, layout verification

Day-2:

- Full custom design flow
 - Pyxis schematic, layout
 - Physical verification using Calibre
- Analog and Mixed signal design and verification
 - Demo on ADMS flow, Mixed simulation & analysis, RC design

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Agenda for two days workshop on VLSI chip design & verification using Mentor Graphics EDA tool:

| DAY-1 | |
|--------------------|--|
| 9:30 – 9:45 | Introduction to CoreEL Technologies |
| 9:45 – 11:00 | Fundamentals of VLSI chip design methodology <ul style="list-style-type: none">• Basics of ASIC & FPGA• Concepts of HDL design and verification for front end• Synthesis technique overview w.r.t. ASIC & FPGA• Details of ASIC foundry & technology• Concepts of DFT and DFT verification |
| 11:00 -11:15 | Tea Break |
| 11:15 – 13:00 | Demo on HDL Design flow for front end <ul style="list-style-type: none">• Hands on Session HDL designer tool flow Simulation using Modelsim/Questasim Synthesis using Leonardo tool |
| Lunch Break | |
| 14:00 – 16:00 | ASIC Semi-custom methodologies <ul style="list-style-type: none">• Hands on session Pyxis Layout• Calculating Area, Timing & Power & optimizing• Layout verification methodologies (DRC,LVS,PEX,DFM,PERC)• Post-layout verification or Back annotation & exporting to GDSII Design for Testability• Layout verification (DRC,LVS,PEX,DFM,PERC) |


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| Day-2 | |
|---------------|--|
| 9:30 – 11:00 | Full Custom Design flow <ul style="list-style-type: none"> • Pyxis Schematic • Pre Layout simulation |
| 11:00 – 11:15 | Tea Break Hands on Session <ul style="list-style-type: none"> • Pyxis Layout • Physical Verification using Calibre(DRC, LVS, Parasitics) • Calibre RVE |
| 13:00 – 14:00 | Lunch <ul style="list-style-type: none"> • Post Layout Simulation(Back annotation) |
| 14:00 – 14:30 | Analog Digital Mixed design & verification <ul style="list-style-type: none"> • Demo on ADMS flow • Mixed simulation & analysis • RC design Guidelines & methodologies |
| 14:30 – 16:30 | Hands on & Q&A Session |

Anslop

Principal

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Mobile : 74830 3119

Fax : 0820-25891

E-mail : ec@sode-e

Website : www.sode-e

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

ATTENDANCE

EVENT: FDP on VLSI Chip Design & Verification using Mentor Graphics EDA Tool

Dates: **22 & 23 Jul 2019** Venue: VLSI Lab, ECE Block, SMVITM

Resource Person: Mr. Vijendra V., Application Engineer, CoreEL Technologies, Bengaluru

| # | Name | Institution | 22/7/19 FN | 22/7/19 AN | 23/7/19 FN | 23/7/19 AN |
|----|-------------------|-------------|------------------------------|------------------------------|------------------------------|------------------------------|
| 1 | CHARISHMA | NMAMIT | Charishma | Charishma | Charishma | Charishma |
| 2 | NIJU RAJAN | NMAMIT | Niju Rajan | Niju Rajan | Niju Rajan | Niju Rajan |
| 3 | MANOJ KUMAR K. | MITK | Manoj Kumar K. | Manoj Kumar K. | Manoj Kumar K. | Manoj Kumar K. |
| 4 | SOOKSHMA ADIGA | MITK | Sookshma Adiga | Sookshma Adiga | Sookshma Adiga | Sookshma Adiga |
| 5 | BALACHANDRA ACHAR | SMVITM | Balachandra Achar | Balachandra Achar | Balachandra Achar | Balachandra Achar |
| 6 | CHETAN R | SMVITM | Chetan R | Chetan R | Chetan R | Chetan R |
| 7 | SOWMYA BHAT | SMVITM | Sowmya Bhat | Sowmya Bhat | Sowmya Bhat | Sowmya Bhat |
| 8 | ARUN UPADHYAYA | SMVITM | Arun Upadhyaya | Arun Upadhyaya | Arun Upadhyaya | Arun Upadhyaya |
| 9 | SHASHIKALA R | SMVITM | Shashikala R | Shashikala R | Shashikala R | Shashikala R |
| 10 | KRISHNA KUMAR | SMVITM | Krishna Kumar | Krishna Kumar | Krishna Kumar | Krishna Kumar |
| 11 | SACHIN PRABHU | SMVITM | Sachin Prabhu | Sachin Prabhu | Sachin Prabhu | Sachin Prabhu |
| 12 | VRUNDA ADKAR | SMVITM | Vrunda Adkar | Vrunda Adkar | Vrunda Adkar | Vrunda Adkar |
| 13 | GANESH SHETTY | SMVITM | Ganesh Shetty | Ganesh Shetty | Ganesh Shetty | Ganesh Shetty |
| 14 | SHAREEN NORONHA | SMVITM | Shareen Noronha | Shareen Noronha | Shareen Noronha | Shareen Noronha |
| 15 | LAXMI SHETTY | SMVITM | Laxmi Shetty | Laxmi Shetty | Laxmi Shetty | Laxmi Shetty |
| 16 | RAJASHREE NAMBIAR | SMVITM | Rajashree Nambiar | Rajashree Nambiar | Rajashree Nambiar | Rajashree Nambiar |
| 17 | SANDESH KUMAR | SMVITM | Sandesh Kumar | Sandesh Kumar | Sandesh Kumar | Sandesh Kumar |
| 18 | RAGHAVENDRA RAO | SMVITM | Raghavendra Rao | Raghavendra Rao | Raghavendra Rao | Raghavendra Rao |
| 19 | AVINASH N. J. | SMVITM | Avinash N. J. | Avinash N. J. | Avinash N. J. | Avinash N. J. |
| 20 | RENITA PINTO | SMVITM | Renita Pinto | Renita Pinto | Renita Pinto | Renita Pinto |

Chetan R
COORDINATOR-1
Chetan R

Sowmya Bhat
COORDINATOR-2
SOWMYA BHAT

Vijendra V
28/7/19
CONVENER

Prasad
Principal
SHRI MADHWA VADIRAJA
INSTITUTE OF TECHNOLOGY & MANAGEMENT
Vishwothama Nagar, Udupi Dist
BANTAKAL - 574 115



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Vishwothamanagar, Bantakal – 574 115, Udupi, Karnataka, India

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Dr. H. V. Balachandra Achar
Professor & Head

23 July 2019

Mr. Vijendra V.
Application Engineer
CoreEL Technologies
Bengaluru

Dear Sir

Subject: **Letter of gratitude**

On behalf of Shri Madhwa Vadiraja Institute of Technology & Management Bantakal, I would like to express our wholehearted thanks to you for conducting a 2-day workshop on the topic "VLSI chip design & verification using Mentor Graphics EDA tool", in the college on 22 & 23 July 2019. The participants were greatly benefitted by the workshop. We look forward for your continued support in the future too.

Thanking you

Balachandra Achar

Principal

SHRI MADHWA VADIRAJA
INSTITUTE OF TECHNOLOGY & MANAGEMENT
Vishwothama Nagar, Udupi Dist.
BANTAKAL - 574 115

Feedback

| Timestamp | The contents of the FDP lived up to my expectations | The presentations were clear and well-organized | The resource person stimulated your interest in the topic | The resource person managed the time well | The hands-on was adequate to learn the topic | The coordinators and lab instructors helped well in case of any difficulties | The food and other hospitality were excellent | What aspects of the FDP were most useful to you? | Any suggestions for improvements in future? |
|------------|---|---|---|---|--|--|---|--|---|
| 2019/07/24 | 4 | 4 | 3 | 3 | 4 | 4 | 4 | 4 content, handson | |
| 2019/07/24 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 Hands-on | Nil |
| 2019/07/24 | 4 | 4 | 5 | 4 | 4 | 5 | 4 | | |
| 2019/07/24 | 4 | 4 | 5 | 4 | 5 | | 4 | | |
| 2019/07/24 | 4 | 3 | 3 | 4 | 4 | 5 | 4 | 4 Placing and | Nil |
| 2019/07/24 | 4 | 4 | 5 | 5 | 5 | 5 | 5 | 5 | |
| 2019/07/24 | 5 | 5 | 5 | 4 | 5 | 5 | 5 | 5 | |
| 2019/07/24 | 4 | 4 | 4 | 3 | 4 | 5 | 5 | 5 hands on | |
| 2019/07/24 | 5 | 5 | 5 | 4 | 5 | 5 | 5 | 5 Full custom | Nil |
| 2019/07/24 | 4 | 4 | 4 | 4 | 4 | 5 | 5 | 5 Full custom design | |
| 2019/07/24 | 5 | 5 | 5 | 4 | 4 | 5 | 5 | 5 Questasim, | Nil |
| 2019/07/24 | 4 | 5 | 4 | 5 | 4 | 5 | 5 | 5 | |
| 2019/07/24 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | |
| 2019/07/24 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 Usage of Leonardo Spec | |
| 2019/07/24 | 5 | 4 | 4 | 4 | 4 | 5 | 4 | 5 Hands-on | |
| 2019/07/26 | 5 | 5 | 5 | 4 | 5 | 5 | 5 | 5 Hands on part was inter | |



Principal

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