COURSE FILE (2022-23)

Department: ELECTRONICS & COMMUNICATION ENGINEERING **Class: 7th Sem**

Course Title: Radar Engineering **Course code: 18EC823**

1. Course details

1.1 Primary information

1	**Course Code**	18EC823
2	**L-T-P**	3-0-0
3	**Course Credit**	3
4	**Marks (Min/Max)** **VTU Exam** **Internal Assessment**	40/100 35/100 16/40
5	**Pre-requisite**	Analog and Digital Communication, Microwave and Antenna

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6	**Teaching Department**	Electronics & Communication Engineering
7	**Course Duration**	40 Hours
8	**Faculty Handling the course**	Mr. Arun Upadhyaya
9	**Course Coordinator**	Mr. Arun Upadhyaya

1.2 Textbooks

1. Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001.

1.3 Reference Books

1. Radar Principles, Technology, Applications — Byron Edde, Pearson Education,2004.
2. Radar Principles – Peebles. Jr, P.Z. Wiley. New York. 1998.
3. Principles of Modem Radar: Basic Principles – Mark A. Rkhards, James A. Scheer, William A. Holm. Yesdee, 2013.

1.4 Other Resources (Online, Text, Multimedia, etc.)

1. https://nptel.ac.in/courses/108/105/108105154/
2. https://ocw.mit.edu/resources/res-ll-001-introduction-to-radar-systems-spring-2007/

1.5 Link of class web page (Google classroom/CANVAS etc.)

https://classroom.google.com/c/NTk2MTk0MTI0ODE2
vtnv6gk

2. Course Plan

2.1 Course Outcomes

Sl. No.	At the end of the course, Students will be able to	Bloom's Level	Target Attainment
CO1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	L3	2.2
CO2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	L3	2.2
CO3	Explain the working and applications of different types of Radar.	L2	2.2
CO4	Describe the working of various radar antennas and receivers.	L2	2.2

Cognitive levels as per Bloom's Taxonomy: L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating and L6-Creating

2.2 Mapping of COs with POs (Course articulation matrix)

	Engineering Knowledge	Problem Analysis	Design &Development of Solutions	Investigations of Complex	Usage of Modern Tools	Engineer & Society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Management & Finance	Life-long Learning		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1							1	3			2	1
CO2	2	1											1	1
CO3	2	1											1	1
CO4	2								1	3			1	

POs Mapping Level: 1-Slightly 2-Moderately 3-Highly

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2.3 Justification for CO-PO mapping

		Justification	Performance Indicator
CO1	PO1	Apply the knowledge of mathematics and engineering fundamentals to derive the equation for radar range.	1.1.1, 1.1.2, 1.3.1, 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems using radar range equation.	2.1.1, 2.1.2, 2.1.3, 2.4.1
	PO9	Demonstrate effective communication skill to explain the concepts like origins of radar and its applications.	9.2.1
	PO10	Read, understand and interpret technical and non-technical information and Deliver effective oral presentations to technical and non-technical audiences by using Use a variety of media effectively to convey a message in a document or presentation to understand concepts like origins of radar and its applications.	10.1.1 10.1.3, 10.2.2, 10.3.1, 10.3.2
	PSO1	Understand the concepts of communication in the field of radar engineering.	--
	PSO2	Apply domain-specific knowledge to understand the use of radar in communication engineering.	--
CO2	PO1	Apply the knowledge of mathematics and engineering fundamentals to determine the impact of noise on radar range equation.	1.1.1, 1.3.1, 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems on modified radar range equation.	2.1.2, 2.1.3 2.2.4, 2.4.1
	PSO1	Apply the concepts of noise in radar communication.	--
	PSO2	Understand the problems related to impact of noise on radar communication.	--
CO3	PO1	Apply the knowledge of mathematics and engineering fundamentals to understand the working and applications of different types of Radar	1.1.1, 1.3.1 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems on Doppler frequency and measurement of speed of targets.	2.1.2, 2.1.3 2.4.1
	PSO1	Understand the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets in radar communication.	--
	PSO2	Understand the problems on Doppler frequency used in radar communication.	--
CO4	PO1	Apply the knowledge of mathematics and engineering fundamentals to understand the working of various radar antennas and receivers.	1.3.1 1.4.1
	PO9	Demonstrate effective communication skill to explain the concepts like types of antennas and receivers.	9.2.1
	PO10	Read, understand and interpret technical and non-technical information and Deliver effective oral presentations to technical and non-technical audiences by using Use a variety of media effectively to convey a message in a document or presentation to understand concepts like types of antennas and receivers.	10.1.1 10.1.3, 10.2.2, 10.3.1, 10.3.2
	PSO1	Understand the use of types of antennas in radar communication systems	--

2.4 Continuous Improvement (Actions taken based on the comments/suggestions of the AY: 2020-21)

SI	Scope for Improvement/Comments/Curriculum Gap (2020-21)	Action Items
1	Most of the topics are covered through Online mode/ Few topics can be covered online mode and remaining through offline	Few topics are covered online mode
2	Need to take more hours to complete the portion	Extra classes taken

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2.5 Topic Level Outcomes

Module	Topic	Topic Level Outcomes (TLO) At the end of the topic, the students will be able to	Blooms Level (L1–L6)	Relevant CO	Assessment Tools
Module-1	**Basics of Radar:** Introduction, Maximum Unambiguous Range, Radar Waveforms, Definitions - PRF, PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. **Simple form of the Radar Equation,** Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar. Illustrative Problems.	**1.1** Understand the working principle of Radar system.	L2	CO1	Internal Assessment /Assignment
		1.2 Define parameters related to Radar system.	L1		
		1.3 Explain simple form of Radar equation.	L3		
		1.4 Explain applications of Radar system and origins of Radar.	L2		
Module-2	**The Radar Equation:** Prediction of Range Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector —Probability of Detection. **Radar Cross Section of Targets:** sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses. Illustrative Problems.	**2.1** Derive the modified equation or radar range with signal to noise ratio.	L2	CO2	Internal Assessment /Assignment
		2.2 Compute probability of detection and false alarm.	L3		
		2.3 Identify different Radar cross section of targets.	L2		
		2.4 Find out transmitter power, pulse repetition frequency and system losses.	L3		
Module-3	**MTI and Pulse Doppler Radar:** Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Delay Line Canceler, MTI Radar with – Power Amplifier Transmitter, Blind Speeds, Clutter Attenuation, MTI Improvement Factor, N- Pulse Delay-Line Canceler, **Digital MTI Processing** – Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector- Original MTD	**3.1** Understand the Principles of MTI and Pulse Doppler Frequency Shift Radars.	L2	CO2	Internal Assessment /Assignment
		3.2 Explain the purpose of delay line canceller and clutter attenuation and derive the frequency response of delay line canceller,	L2		
		3.3 Describe the working of Digital MTI Processing and moving target detectors.	L2		
Module-4	**Tracking Radar:** Tracking with Radar-Types of Tracking Radar Systems, Monopulse Tracking- Amplitude Comparison Monopulse (one-and two-coordinates), and Phase Comparison	**4.1** Understand the types of Tracking Radar Systems.	L2	CO3	Internal Assessment /Assignment
		4.2 Describe mono-pulse tracking.	L2		

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	Monopulse. **Sequential Lobing**, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range, Comparison of Trackers.	**4.3** Explain Conical Scan Tracking Radar.	L2		
Module-5	**The Radar Antenna:** Functions of The Radar Antenna, Antenna Parameters, Reflector Antennas and Electronically Steered Phased array Antennas. The Radar Receiver, Receiver Noise Figure, Super Heterodyne Receiver, Duplexers and Receivers Protectors, Radar Displays.	**5.1** Different functions served by Radar antenna and types of antennas used in radar.	L2	**CO4**	Internal Assessment /Assignment
		5.2 Understand the Radar receiver and role of duplexer's in Radar system.	L2		
		5.3 Explain different types of Radar display systems, receiver protectors	L2		

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2.6 Course Delivery Schedule

Lect. /Tut No.	Topics to be covered	Relevant TLO	Date on which topics covered	Mode of Delivery	Faculty Sign (Every class)	HoD Sign (Every Module)
	Module 1					
L1	Basics of Radar: Introduction, Maximum Unambiguous Range	1.1	17/2	BB		
L2	Radar Waveforms, Definitions with respect to pulse waveform - PRF, PRI,	1.2	17/2	BB		
L3	Definitions with respect to pulse waveform - Duty Cycle, Peak Transmitter Power, Average transmitter Power.	1.2	3/3	BB		
L4	Illustrative Problems	1.2	3/3	BB		
L5	Simple form of the Radar Equation,	1.3	4/3	BB		
L6	Radar Block Diagram and Operation, Radar Frequencies	1.1	10/3	BB		
L7	Illustrative Problems	1.3	10/3	BB		
L8	Applications of Radar, The Origins of Radar	1.4	10/3	Seminar		
	Module 2					
L9	The Radar Equation: Prediction of Range Performance,	2.1	11/3	BB PPT		
L10	Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR,	2.1	17/3	BB PPT		
L11	Modified Radar Range Equation	2.2	17/3	BB		
L12	Envelope Detector — False Alarm Time and Probability	2.2	24/3	BB PPT		
L13	Probability of Detection	2.2	24/3	BB		
L14	simple targets – sphere, cone-sphere, Transmitter Power	2.3	24/3	BB PPT		
L15	PRF and Range Ambiguities, System Losses	2.4	25/3	BB		
L16	Illustrative Problems	2.2	25/3	BB		
	Module 3					
L17	MTI and Pulse Doppler Radar: Introduction, Principle	3.1	6/4	BB		
L18	Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction	3.1	6/4	BB		

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L19	Delay Line Canceler, MTI Radar with – Power Amplifier Transmitter	3.2	6/4	BB		
L20	Delay Line Cancelers — Frequency Response of Single Delay- Line Canceler	3.2	8/4	BB		
L21	Blind Speeds, Clutter Attenuation, MTI Improvement Factor	3.2	8/4	BB		
L22	N- Pulse Delay-Line Canceler,	3.2	10/4	BB		
L23	Digital MTI Processing – Blind phases, I and Q Channels	3.3	10/4	BB		
L24	Digital MTI Doppler signal processor, Moving Target Detector- Original MTD	3.3	10/4	BB		
	Module 4					
L25	Tracking Radar: Tracking with Radar- Types of Tracking Radar Systems	4.1	13/4	BB PPT		
L26	Monopulse Tracking-Amplitude Comparison Monopulse	4.2	13/4	BB PPT		
L26	Phase Comparison Monopulse.	4.2	17/4	BB		
L28	Sequential Lobing	4.3	17/4	BB		
L29	Conical Scan Tracking	4.3	24/4	BB		
L30	Block Diagram of Conical Scan Tracking Radar	4.3	24/4	BB		
L31	Tracking in Range	4.3	25/4	BB		
L32	Comparison of Trackers.	4.3	25/4	BB		
	Module 5					
L33	The Radar Antenna: Functions of The Radar Antenna	5.1	6/5	Seminar		
L34	Antenna Parameters, Reflector Antennas	5.1	6/5	Seminar		
L35	Electronically Steered Phased array Antennas	5.1	6/5	Seminar		
L36	The Radar Receiver, Receiver Noise Figure	5.2	7/5	Seminar		
L37	Super Heterodyne Receiver	5.2	7/5	Seminar		
L38	Duplexers	5.2	7/5	Seminar		
L39	Radar Displays	5.3	7/5	Seminar		
L40	Receivers Protectors	5.3	7/5	Seminar		

Signature of Faculty Handling/ Course Coordinator/Module Coordinator Date: 17/2

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HOD Date: 26/06/23

2.7 Topics Covered Beyond Syllabus

Date	Topic Covered	Relevant PO	Mode of delivery
10/3	Real time application of Radar	PO1	PPT/Seminar
7/5	Radar Displays with real time images	PO1	PPT/Seminar

2.8 Remedial class Details

S. No.	Date	Topic discussed/numerical problem solved	No. of Students attended
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2.9 Innovative teaching methods adapted

S. No.	Date	Innovative method adapted	Topics covered
1	8/04/2023	Flipped Class Room	Frequency Response of Single DLC and Blind Speed
2	8/04/2023	Flipped Class Room	N-Pulse DLC
3	24/04/2023	Flipped Class Room	Conical Scanning & Sequential Lobing
4	13/04/2023	Flipped Class Room	Monopulse Tracking

3. Assessment of COs

3.1 Assessment Schedule

Date	Assessment Tool Used	TLOs Assessed	Average Cognitive Level
31/03/2023	IA-1	1.1,1.2,1.3, 1.4, 2.1, 2.2, 2.3, 2.4	2.42
20/04/2023	IA-2	3.1, 3.2, 3.3	2.53
11/05/2023	IA-3	4.1, 4.2, 4.3, 5.1, 5.2, 5.3	2.00

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3.2 Measuring CO Attainment

3.2.1 Direct attainment

TLOs mapped	Assessment Tool Used	Attained Level of Bloom's Taxonomy	Marks allotted	Total Marks	Weightage	Attainment Level	Contribution to CO Attainment	CO - Direct attainment
1.1	IA1	L2	7	30	0.23	3	0.7	1.40
1.2	IA1	L2	8		0.27	0	0	
1.3	IA1	L3	8		0.27	0	0	
1.4	IA1	L2	7		0.23	3	0.7	
2.1	IA1	L3	8	30	0.27	1	0.27	2.07
2.2	IA1	L3	12		0.40	3	1.2	
2.3	IA1	L2	6		0.20	1	0.2	
2.4	IA1	L2	4		0.13	3	0.4	
3.1	IA2	L3	38	90	0.42	3	1.27	2.60
3.2	IA2	L3	16		0.18	2	0.36	
3.3	IA2	L2	6		0.07	3	0.2	
4.1	IA3	L2	7		0.08	0	0	
4.2	IA3	L2	8		0.09	3	0.27	
4.3	IA3	L2	15		0.17	3	0.5	
5.1	IA3	L2	7	30	0.23	0	0	2.30
5.2	IA3	L2	8		0.27	3	0.8	
5.3	IA3	L2	15		0.50	3	1.5	

3.2.2 Indirect attainment (Course end survey)

S. No.	CO questions	Number of students responded			Indirect Attainment Level (3*A+2*B+C)/N
		Strongly agree (A)	Agree (B)	Neutral (C)	
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	5	3	0	2.333333333
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2	6	0	2
3	Explain the working and applications of different types of Radar.	1	7	0	1.888888889
4	Describe the working of various radar antennas and receivers.	1	7	0	1.888888889

3.2.3 Final CO attainment

Sl. No.	Course Outcomes	Direct attainment	Indirect attainment	Final CO = 80% DA + 20% IA
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	1.4	2.333333333	**1.59**
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2.07	2	**2.06**

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3	Explain the working and applications of different types of Radar.	2.6	1.888888889	**2.46**
4	Describe the working of various radar antennas and receivers.	2.3	1.888888889	**2.22**

3.3 Observations of Course coordinator on CO attainment

Sl. No.	Course Outcomes	Target	Attainment	Gap	Action Proposed to bridge the Gap	Revision of target wherever achieved
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	2.2	1.59	0.61	Students should be engaged through online class	2.2
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2.2	2.06	0.14	Students should be engaged through online class	2.2
3	Explain the working and applications of different types of Radar.	2.2	2.46	-	-	2.3
4	Describe the working of various radar antennas and receivers.	2.2	2.22		-	2.3

3.4 Other Information

	Section - A
Total number of classes held	40
Number of tutorial classes held	-
Number of seminars held	12
Portion coverage	100
Student's feedback	-
No. of students having attendance shortage	-
University result	100
Use of various teaching methods	Black Board, PPT, Video, Google Classroom
Details of the e-content developed	PPT- 32, YouTube Videos – 09 Google Classroom

3.5 Outcomes on Actions of the Observations/Suggestions of the AY: 2021-22

S. No.	Action Taken	Change Observed
1	Seminar were conducted	More Student involvement
2	Innovative teaching methods used	Students understood the topic well

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3.6 Comments/Suggestions by the Course Coordinator for the next academic year

S. No.	Comment/Observations	Suggested Actions
1	Many Students missed classes due internships opportunities	Students can be engaged through online class.
2	—	---

Remarks by the Module Coordinator CO1 & CO2 target to be retained and revision of CO's are suggested for CO3 & CO4

Signature of Faculty Handling/Course Coordinator/Module Coordinator
Date: 26/6/23

HOD
Date: 26/6/23

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Vishwothama Nagar, Udupi Dist.
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Department: ECE	IA- I	Academic Year: 2021-22
Class: V semester	Course: Verilog HDL	Course Code: 18EC56
Date: 22/11/2021	Duration: 75 minutes	Max. Marks: 30

QP Version: A

Note: Answer the following questions

Qn. No	Question	Marks	PI*	BL*	CO*
1(a)	Explain the typical design flow for designing VLSI IC Circuits.	6	1.3.1	L2	CO1
(b)	Illustrate top-down design methodology with the help of 4-bit ripple counter module.	6	1.4.1	L3	CO1
	OR				
2(a)	Discuss the different levels of abstraction used in Verilog modeling.	6	1.4.1	L2	CO1
(b)	With the help of block diagram, truth table, necessary equations, design block code and stimulus code, implement 2:4 decoder using basic gates.	6	1.3.1	L3	CO1
3(a)	Illustrate the different gates supported by Verilog HDL with the help of truth table consisting of input values '0', '1', 'X' and 'Z'. Also write the Verilog HDL statements to instantiate all the gates.	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A circuit rings a bell whenever motion is detected from one of the two motion sensors. A switch S determines which sensor to pay attention to: S=0 => ring the bell when there's motion at motion sensor 1 S=1 => ring the bell when there's motion at motion sensor 2	6	1.3.1	L4	CO3
(c)	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	6	1.4.1	L3	CO1
	OR				
4(a)	Write gate level description to implement function y= (a. b) +c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	6	1.3.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A car has a fuel-level detector that outputs the current fuel-level as a 3-bit binary number, with 000 meaning empty and 111 meaning full. Using the combinational design process, create a circuit that illuminates a "low fuel" indicator light (by setting an output L to 1) when the fuel level drops below level 3.	6	1.3.1	L4	CO3
(c)	Implement the below problem statement in dataflow modeling. Let variables T represent being tall, H being heavy, and F being fast. Let's consider anyone who is not tall as short, not heavy as light, and not fast as slow. a. You may ride a particular amusement park ride only if you are either tall and light, or short and heavy. b. You may NOT ride an amusement park ride if you are either tall and light, or short and heavy. c. You are eligible to play on a particular basketball team if you are tall and fast, or tall and slow.	6	1.4.1	L3	CO3

BL* Bloom's Taxonomy Level; CO* Course Outcome; PI- Performance Indicator

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QP quality

CO	Maximum Marks	Maximum marks			% questions		
		L2 level questions	L3 level questions	L4 level questions	L2 level questions	L3 level questions	L4 level questions
CO1	30	12	18	0	20	30	0
CO3	30	0	18	12	0	30	20

Overall QP quality = 2 X % of L2 questions + 3 X % of L3 questions + 4 X % of L4 questions
= (2 X 0.2) + (3 X 0.6) + (4 X 0.2)
= 3

Prepared By (Name & signature with date): Ms. Sowmya Bhat
13/11/2021

Remarks by scrutiny team:
Course type (Theoretical/Theoretical & numerical/Numerical)

Scrutinized by (Name & signature with date): HVB Achar
15/11/21

QP selected for the test: YES/NO

HoD Signature with date and seal

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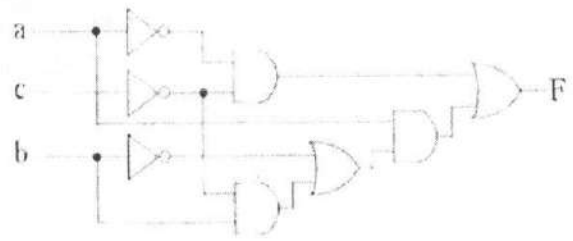
SMVITM

Department: ECE	IA- I	Academic Year: 2021-22
Class: V semester	Course: Verilog HDL	Course Code: 18EC56
Date: 22/11/2021	Duration: 75 minutes	Max. Marks: 30

QP Version: B

Note: Answer the following questions

Qn. No	Question	Marks	PI*	BL*	CO*
1(a)	Explain design flow for designing VLSI IC circuits with a neat flowchart.	6	1.3.1	L2	CO1
(b)	Illustrate bottom-down design methodology with the help of 4-bit ripple counter module.	6	1.4.1	L3	CO1
	OR				
2(a)	Discuss the different components of a simulation used in Verilog modeling.	6	1.4.1	L2	CO1
(b)	With the help of block diagram, truth table, necessary equations, design block code and stimulus code, implement 4:1 Multiplexer using basic gates.	6	1.3.1	L3	CO1
3(a)	Illustrate the different gates supported by Verilog HDL with the help of truth table consisting of input values '0', '1', 'X' and 'Z'. Also write the Verilog HDL statements to instantiate all the gates.	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A museum has three rooms, each with a motion sensor (m0, m1, and m2) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks from room to room. Create a circuit that sounds an alarm (by setting an output A to 1) if motion is ever detected in more than one room at a time (i.e., in two or three rooms), meaning there must be one or more intruders in the museum.	6	1.3.1	L4	CO3
(c)	Let variables S represent a package being small, H being heavy, and E being expensive. Consider a package that is not small as big, not heavy as light, and not expensive as inexpensive. Implement the below problem statement in dataflow modeling. a. You can deliver packages only if the packages are either small and expensive, or big and inexpensive. b. You can NOT deliver a package only if the packages are either small and expensive, or big and inexpensive. c. You can load the packages into your truck only if the packages are small and light, small and heavy, or big and light.	6	1.4.1	L3	CO3
	OR				
4(a)	Implement the below circuit in gate level modeling. 	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A house has four external doors each with a sensor that outputs 1 if its door is open. Inside the house is a single LED that a homeowner wishes to use to indicate whether a door is open or closed. Because the LED can only show the status of one sensor, the homeowner buys a switch that can be set to 0, 1, 2, or 3 and that has a 2-bit output.	6	1.3.1	L4	CO3

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	representing the switch position in binary. Create a circuit to connect the four sensors, the switch, and the LED.			
(c)	Write gate level description to implement function y=a+(b.c), with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	6	L3	CO2

BL* Bloom's Taxonomy Level; CO* Course Outcome; PI- Performance Indicator

QP quality

CO	Maximum Marks	Maximum marks			% questions		
		L2 level questions	L3 level questions	L4 level questions	L2 level questions	L3 level questions	L4 level questions
CO1	30	12	18	0	20	30	0
CO2	30	0	18	12	0	30	20

Overall QP quality = 2 X % of L2 questions + 3 X % of L3 questions + 4 X % of L4 questions
= (2 X 0.2) + (3 X 0.6) + (4 X 0.2)
= 3

Prepared By (Name & signature with date): Ms. Sowmya Bhat
13/11/2021

Remarks by scrutiny team:
Course type (Theoretical/Theoretical & numerical/Numerical)

Scrutinized by (Name & signature with date): HVB Achar
15/11/21

QP selected for the test: YES/NO

HoD Signature with date and seal

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CBCS SCHEME

USN | | | | | | | | | | BESCK104C/ BESCKC104

First Semester B.E./B.Tech. Degree Examination, Jan./Feb. 2023
Introduction to Electronics and Communication

Time: 3 hrs. Max. Marks: 100

Note: 1. *Answer any FIVE full questions, choosing ONE full question from each module.*
2. *VTU Formula Hand Book is permitted.*
3. *M : Marks , L: Bloom's level , C: Course outcomes.*

		Module – 1	M	L	C
Q.1	a.	Draw the block diagram of DC power supply and explain the individual blocks.	8	L2	CO1
	b.	Draw the circuit diagram of voltage regulation and explain the operation.	6	L2	CO1
	c.	An amplifier produces an output voltage of 2V for an input of 50mV. If the input and output currents in this condition are 1mA and 200mA respectively. Find : i) The voltage gain ii) The current gain iii) The power gain.	6	L3	CO1
		OR			
Q.2	a.	With a neat circuit diagram and waveform Explain the working operation of a full wave bridge rectifier.	8	L2	CO1
	b.	Draw the circuit diagram of voltage doubler and the working operation.	6	L2	CO1
	c.	Discuss briefly a Negative feedback amplifier with block diagram.	6	L1	CO1
		Module – 2			
Q.3	a.	With circuit diagram, explain the operation of an wien bridge oscillator.	8	L2	CO2
	b.	Define the following operational amplifier parameters value. i) Open loop voltage gain ii) Output Resistance iii) Slew Rate	6	L1	CO2
	c.	Draw the circuit diagram and input and output waveform of the following operational amplifier circuits i) Differentiators ii) Integrator.	6	L1	CO2
		OR			
Q.4	a.	Explain the single state astable oscillator with circuit diagram.	8	L1	CO2
	b.	What is oscillator? And mention condition for oscillations.	6	L1	CO2
	c.	Explain the operation of summing amplifier using operational amplifier and write the output equation.	6	L2	CO2

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		Module – 3			
Q.5	a.	Implement full adder using two half adders and one OR gate. Write the equations for Sum and C_{out}.	8	L3	CO3
	b.	Convert the following numbers to its equivalent numbers and show the steps. i) $(10110001101011.111100000)_2 = (?)_8$ ii) $(10110001101011.11110010)_2 = (?)_{16}$ iii) $(1010.011)_2 = (?)_{10}$	6	L2	CO3
	c.	Using basic Boolean theorems prove i) $(x + y)(x + z) = x + yz$ ii) $xy + xz + y\bar{z} = xz + y\bar{z}$	6	L3	CO3
		OR			
Q.6	a.	Express the Boolean function i) $F = A + \bar{B}C$ in a sum of minterms form ii) $F = xy + \bar{x}z$ in a product of maxterms form.	8	L2	CO3
	b.	Subtract the following using 10's complement i) $(72532 - 3250)_{10}$ ii) $(3250 - 72532)_{10}$	6	L2	CO3
	c.	Write the step by step procedure to design a combinational circuit.	6	L1	CO3
		Module – 4			
Q.7	a.	What is an Embedded system? Compare Embedded systems with general computer systems.	8	L2	CO4
	b.	Mention the classification of Embedded system based on complexity and performance.	6	L1	CO4
	c.	Write a short note on – 7-segment LED display.	6	L2	CO4
		OR			
Q.8	a.	Discuss the typical embedded system elements.	8	L2	CO4
	b.	What is the difference between RISC and CISC processors?	6	L1	CO4
	c.	Write a short note on : i) Transducers ii) Sensors.	6	L2	CO4
		Module – 5			
Q.9	a.	Draw the block diagram of basic communication system and briefly explain the individual blocks.	10	L2	CO5
	b.	Discuss the types of communication systems.	5	L2	CO5
	c.	List the advantages of digital communication over analog communication.	5	L1	CO5
		OR			
Q.10	a.	Define Amplitude and Frequency modulation. Sketch AM and FM waveform.	10	L1	CO5
	b.	Write a short note on : Amplitude Shift Keying (ASK) modulator and demodulator.	10	L2	CO5

* * * * *

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(Affiliated to Visvesvaraya Technological University, Belagavi)
Vishwothama Nagar, Bantakal – 574115, Udupi District, Karnataka

SMVITM

IPCC BEC302 - Digital System Design using Verilog LAB

LABORATORY MANUAL

IVTH SEMESTER B.E. (ECE)

NAME OF THE STUDENT : _____

UNIVERSITY SEAT NUMBER : _____

SECTION & BATCH : _____

Prepared by: Ms Sowmya Bhat

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Department Vision:

To be recognized as a center of eminence in the field of Electronics and Communication Engineering for holistic engineering education and research on current technologies.

Department Mission:

1. Impart quality engineering education with ethics to students and transform them into leaders in technology, innovation and research.
2. Provide a platform and academic atmosphere that will ensure the transfer of knowledge and skills to the students.
3. Promote the overall personality development of the students through activities that have high credibility and societal impact.

Programme Educational Objectives:

The graduate of Electronics and Communication Engineering should be able to

PEO-1 Exhibit essential knowledge of applied sciences, mathematical modelling, logical interpretation and virtual realization to resolve real-time problems in the field of Electronics and Communication Engineering

PEO-2 Work productively as an Electronics and Communication Engineer, including supportive and leadership roles on multidisciplinary teams.

PEO-3 Inculcate effective communication skills to excel in professional growth.

PEO-4 Take part in lifelong learning in pace with the advancing technological society.

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DIGITAL SYSTEM DESIGN USING VERILOG LAB

B.E., III Semester, Electronics & Communication Engineering

2022 Scheme

Course Code	BEC302	**CIE Marks**	25
Exam duration	2/3 hours		

Course Objectives

This course will enable the students to:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

S.No.	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder, 2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type
8	To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

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Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D,T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.

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- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

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TABLE OF CONTENTS

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3. Fundamentals of HDL,by Cyril PR, Pearson/Sanguine2010

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Experiment No: 1

AIM: To simplify the given Boolean expressions and realize using Verilog program

Y1= A′ B′ + AB + A′ B

Y2= (A + B) (A + B′)

Y3= A′ B + AB′ + A′ B′ +AB

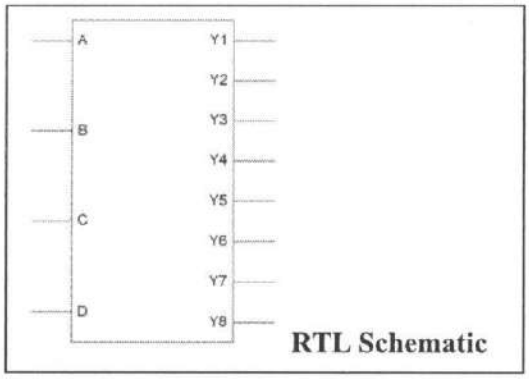
Y4= AB′ + B′ C′ + A′ C′

Y5= A′ BC + AC

Y6= AB + A (CD + CD′)

Y7= (BC′ + A′ D) (AB′ + CD′)

Y8=A′ BC + AB′ C′ + A′ B′ C′ +ABC



RTL Schematic

Top Module Program for Boolean Expression

```
module bool (A, B, C, D, Y1, Y2, Y3, Y4, Y5,
Y6, Y7, Y8);
input A,B,C,D;
output Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
assign Y1= ~A | B;
assign Y2= A;
assign Y3= 1;
assign Y4= (A& (~B)) | ((~A) & (~C));
assign Y5= C & (A | B);
assign Y6= A & (B | C);
assign Y7= 0;
assign Y8= (B & C) | ((~B) & (~C));
endmodule
```

Testbench Code for Boolean Expression

```
module bool_test;
reg A, B, C, D;
wire Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8;
bool uut (.A(A),.B(B),.C(C),.D(D),
.Y1(Y1), .Y2(Y2), .Y3(Y3), .Y4(Y4),
.Y5(Y5), .Y6(Y6), .Y7(Y7), .Y8(Y8) );
initial
begin
A=0; B=0; C=0; D=0;
end
always
begin
#10 D=!D;
#20 C=!C;
#40 B=!B;
#80 A=!A;
end
initial
begin
#100 $finish;
end
endmodule
```

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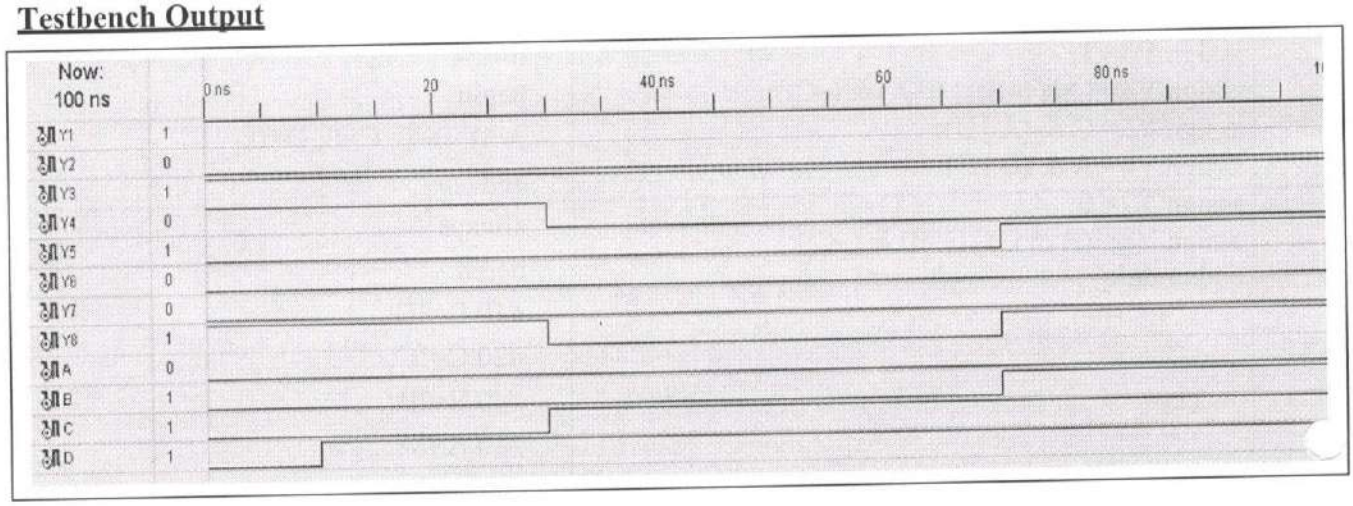
Truth Table

Inputs				Outputs							
A	B	C	D	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	1	0	1	1	0	0	0	1
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	1	0	1	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	0
0	1	0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	1	0	1	0	1	0	0	1
0	1	1	1	1	0	1	0	1	0	0	1
1	0	0	0	0	1	1	1	0	0	0	1
1	0	0	1	0	1	1	1	0	0	0	1
1	0	1	0	0	1	1	1	1	1	0	0
1	0	1	1	0	1	1	1	1	1	0	0
1	1	0	0	1	1	1	0	0	1	0	0
1	1	0	1	1	1	1	0	0	1	0	0
1	1	1	0	1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	0	1	1	0	1

Testbench Output



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Experiment No: 2

AIM: To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.

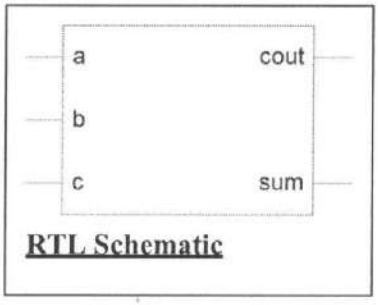
Top Module Code for Full Adder

```
module fulladder (sum,cout, a, b, c);
output sum, cout;
input a, b,c;
assign sum= a ^ b ^ c;
assign cout= (a & b) | (b & c) | (c & a);
endmodule
```

Testbench Code for Full Adder

```
module fulladder_test;
reg a,b,c;
wire sum,cout;
fulladder uut
(.a(a),.b(b),.c(c),.sum(sum),.cout(cout));
initial
begin
a=0;b=0;c=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
always
#5 c=!c;
initial

begin
#100 $finish;
end
endmodule
```



RTL Schematic

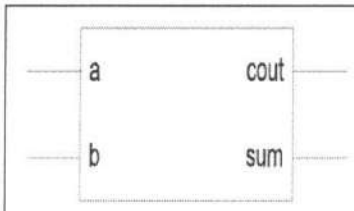
Top Module Code for Half Adder

```
module halfadder (sum,cout, a, b);
output sum, cout;
input a, b;
assign sum= a ^ b;
assign cout= (a & b);
endmodule
```

Testbench Code for Half Adder

```
module halfadder_test;
reg a,b;
wire sum,cout;
halfadder uut
(.a(a),.b(b),.sum(sum),.cout(cout));
initial
begin
a=0;b=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
initial

begin
#100 $finish;
end
endmodule
```



RTL Schematic

Top Module Code for Full Subtractor

```
module fullsubtractor (diff,bout, a, b, bin);
output diff, bout;
input a, b,bin;
assign diff= a ^ b ^ bin;
assign bout= (~a & bin) | (~a & b) | (b &
bin);
endmodule
```

Top Module Code for Half Subtractor

```
module halfsubtractor (diff,bout, a,
b);
output diff,bout;
input a, b;
assign diff= a ^ b;
assign bout= (~a & b);
```

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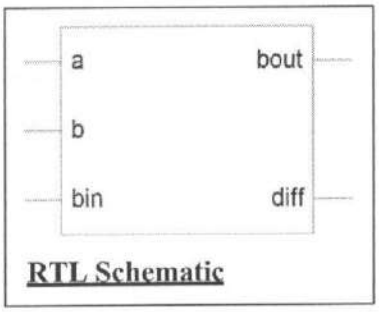
	endmodule

Testbench Code for Full Subtractor

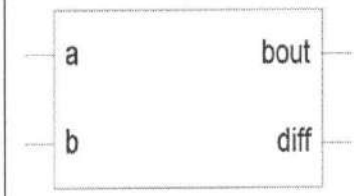
```
module fullsubtractor_test;
reg a,b,bin;
wire diff, bout;
fullsubtractor uut
(.a(a),.b(b),.bin(bin),.diff(diff),.bout(bout));
initial
begin
a=0;b=0;bin=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
always
#5 bin=!bin;
initial
begin
#100 $finish;
end
endmodule
```



RTL Schematic

Testbench Code for Half Subtractor

```
module halfsubtractor_test;
reg a,b;
wire diff, bout;
halfsubtractor uut
(.a(a),.b(b),.diff(diff),.bout(bout));
initial
begin
a=0;b=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
initial
begin
#100 $finish;
end
endmodule
```



RTL Schematic

Truth Table

Inputs		Half Adder Outputs		Half Subtractor Outputs	
a	b	cout	sum	bout	diff
0	0	0	0	0	0
0	1	0	1	1	1
1	0	0	1	0	1
1	1	1	0	0	0

Inputs			Full Adder Outputs		Full Subtractor Outputs	
a	b	c/bin	cout	sum	bout	diff
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	1	1	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

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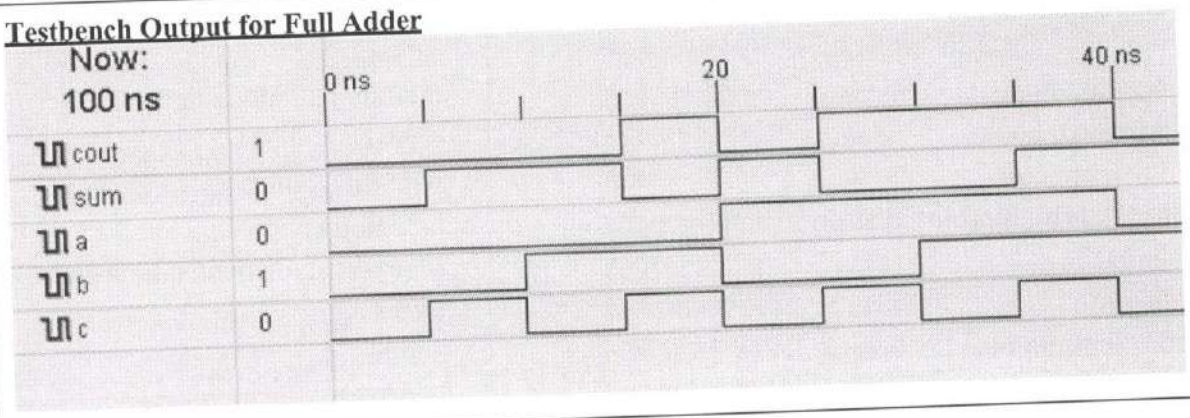
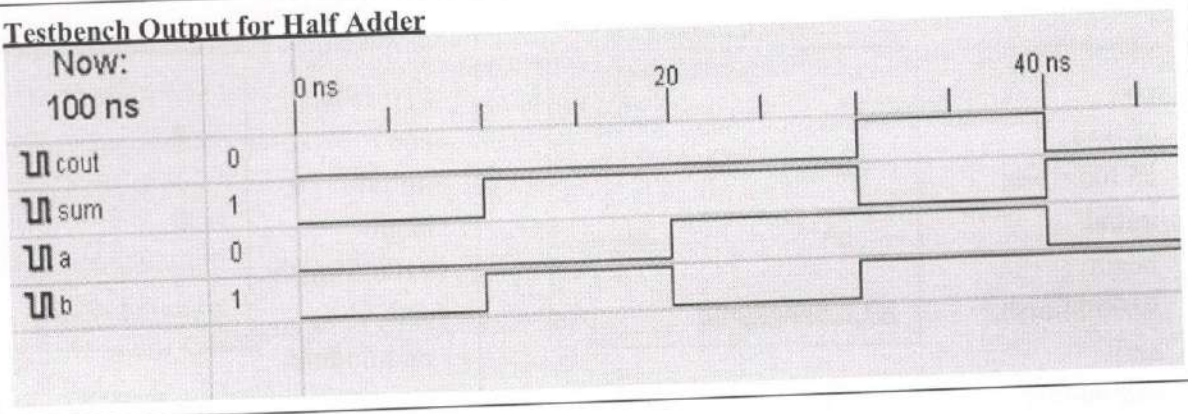
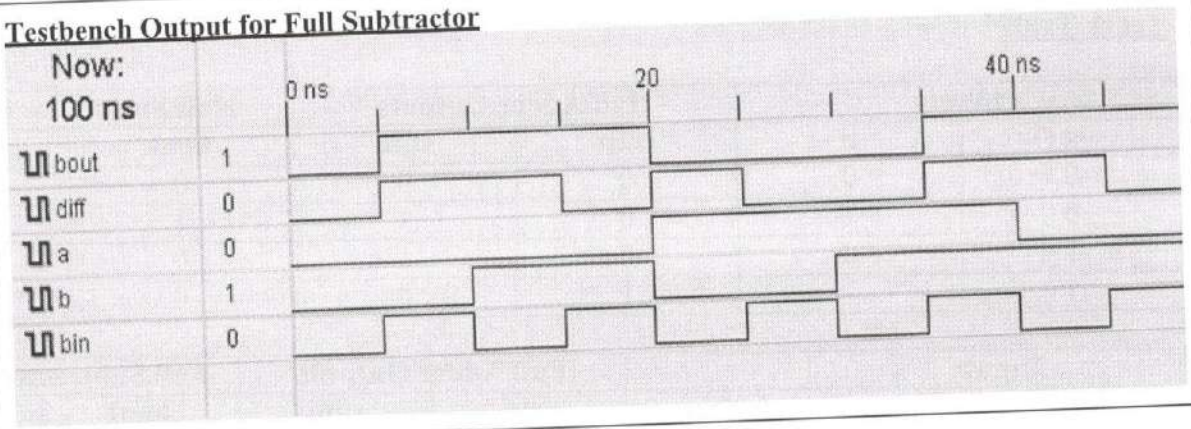
Testbench Output for Full Adder



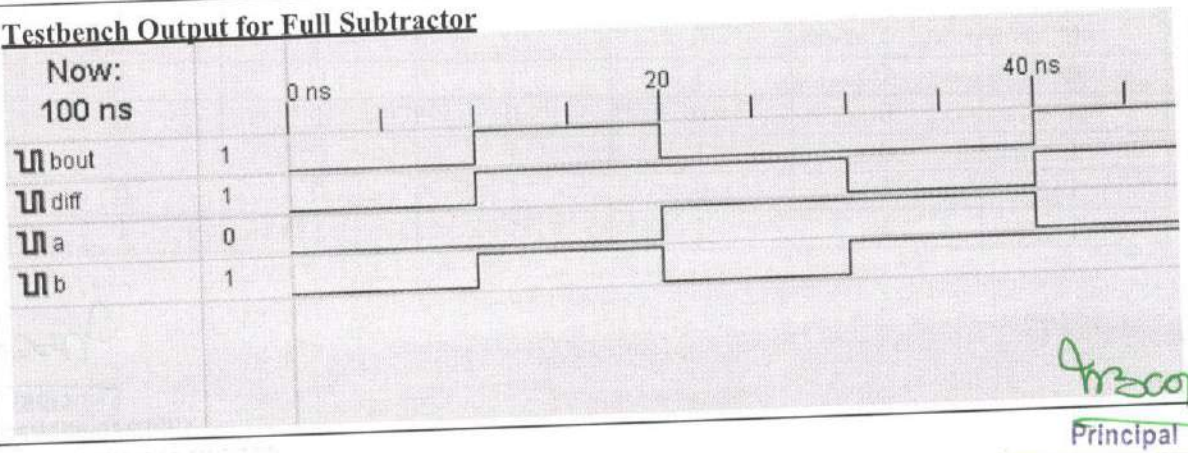
Testbench Output for Half Adder



Testbench Output for Full Subtractor



Testbench Output for Full Subtractor



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Experiment No: 3

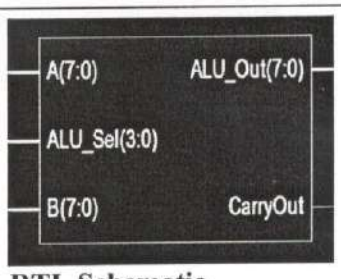
AIM: To realize 4-bit ALU using Verilog program.

Top Module Code for 4-bit ALU

```
module alu(A,B, ALU_Sel, ALU_Out,
CarryOut);
input [7:0] A, B;
input [3:0] ALU_Sel;
output [7:0] ALU_Out;
output CarryOut;
reg [7:0] ALU_Result;
wire [8:0] tmp;
assign ALU_Out = ALU_Result;
assign tmp = {1'b0,A} + {1'b0,B};
assign CarryOut = tmp[8];
always @ (ALU_Sel)
begin
case (ALU_Sel)
4'b0000: ALU_Result = A + B;
4'b0001: ALU_Result = A - B;
4'b0010: ALU_Result = A * B;
4'b0011: ALU_Result = ~A;
4'b0100: ALU_Result = A<<1;
4'b0101: ALU_Result = A>>1;
4'b0110: ALU_Result = {A [6:0], A [7]};
4'b0111: ALU_Result = {A [0], A [7:1]};
4'b1000: ALU_Result = A & B;
4'b1001: ALU_Result = A | B;
4'b1010: ALU_Result = A ^ B;
4'b1011: ALU_Result = ~ (A | B);
4'b1100: ALU_Result = ~ (A & B);
4'b1101: ALU_Result = ~ (A ^ B);
4'b1110: ALU_Result = (A>B)?8'd1:8'd0;
4'b1111: ALU_Result = (A==B)?8'd1:8'd0;
default: ALU_Result = A + B;
endcase
end
endmodule
```

Testbench Code for 4-bit ALU

```
module alu_test;
reg [7:0] A, B;
reg [3:0] ALU_Sel;
wire [7:0] ALU_Out;
wire CarryOut;
alu uut(.A(A),
.B(B),.ALU_Sel(ALU_Sel),.ALU_Out(ALU_Out),
.CarryOut(CarryOut));
initial
begin
A=8'b10101011; B=8'b01010101;
ALU_Sel =4'b0000; #5;
ALU_Sel =4'b0001; #5;
ALU_Sel =4'b0010; #5;
ALU_Sel =4'b0011; #5;
ALU_Sel =4'b0100; #5;
ALU_Sel =4'b0101; #5;
ALU_Sel =4'b0110; #5;
ALU_Sel =4'b0111; #5;
ALU_Sel =4'b1000; #5;
ALU_Sel =4'b1001; #5;
ALU_Sel =4'b1010; #5;
ALU_Sel =4'b1011; #5;
ALU_Sel =4'b1100; #5;
ALU_Sel =4'b1101; #5;
ALU_Sel =4'b1110; #5;
ALU_Sel =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```



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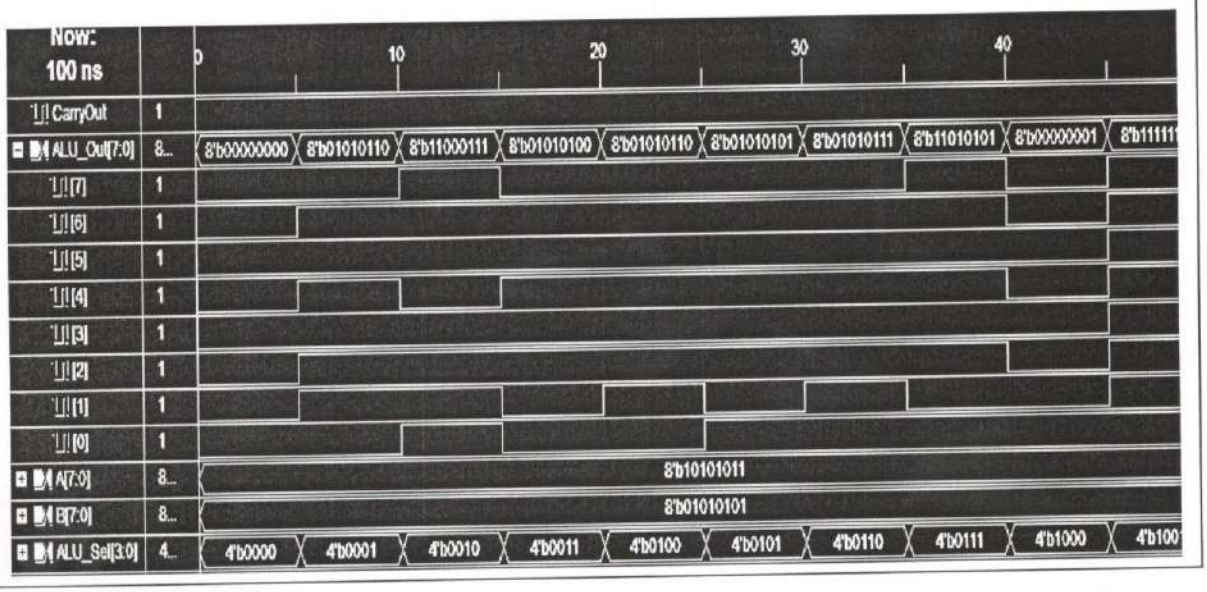
Opcode

ALU_Sel	ALU_Result
0000	A + B - Addition
0001	A – B - Subtraction
0010	A * B - Mutiplication
0011	~A - Complement
0100	A<<1 – logical shift left
0101	A>>1 – logical shift right
0110	{A [6:0], A [7]} – Rotate left
0111	{A [0], A [7:1]} – Rotate right
1000	A & B – logical AND
1001	A | B – logical OR
1010	A ^ B – logical EXOR
1011	~ (A | B) – logical NOR
1100	~ (A & B) – logical NAND
1101	~ (A ^ B) – logical EXNOR
1110	(A>B)?8'd1:8'd0 – greater comparison
1111	(A==B)?8'd1:8'd0 – equal comparison
default	A + B

Testbench Output for 4-bit ALU



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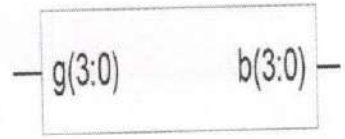
Experiment No: 4

AIM: To realize the following Code converters using Verilog Behavioral description

a) Gray to binary and vice versa b) Binary to excess3 and vice versa

Top Module Code for Gray to Binary

```
module gray_to_binary (g,b);
input [3:0] g;
output [3:0] b;
reg [3:0] b;
always@(g)
begin
b[3] =g[3];
b[2] =b[3] ^ g[2];
b[1] =b[2] ^ g[1];
b[0] =b[1] ^ g[0];
end
endmodule
```



RTL Schematic

Testbench Code for Gray to Binary

```
module gray_to_binary_test;
reg [3:0] g;
wire [3:0] b;
gray_to_binary uut(.g(g), .b(b));
initial
begin
g =4'b0000; #5;
g =4'b0001; #5;
g =4'b0010; #5;
g =4'b0011; #5;
g =4'b0100; #5;
g =4'b0101; #5;
g =4'b0110; #5;
g =4'b0111; #5;
g =4'b1000; #5;
g =4'b1001; #5;
g =4'b1010; #5;
g =4'b1011; #5;
g =4'b1100; #5;
g =4'b1101; #5;
g =4'b1110; #5;
g =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

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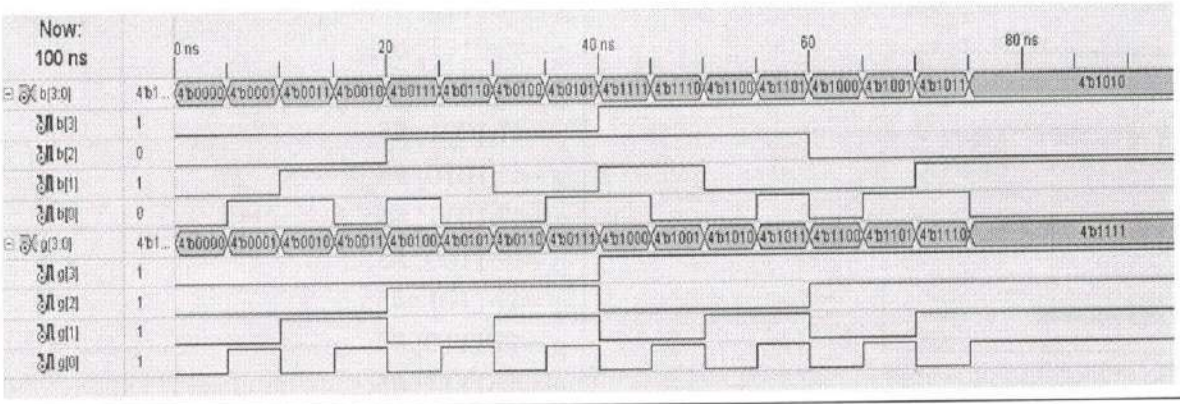
Truth Table

Inputs				Outputs			
g3	g2	g1	g0	b3	b2	b1	b0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Testbench Output for Gray to Binary



Top Module Code for Binary to Gray

```
module binary_to_gray (b, g);
input [3:0] b;
output [3:0] g;
reg [3:0] g;
always@(b)
begin
g[3] = b[3];
g[2] = b[3] ^ b[2];
g[1] = b[2] ^ b[1];
g[0] = b[1] ^ b[0];
end
endmodule
```

Testbench Code for Binary to Gray

```
module binary_to_gray _test;
reg [3:0] b;
wire [3:0] g;
binary_to_gray  uut(.b(b), .g(g));
initial
begin
b =4'b0000; #5;
b =4'b0001; #5;
b =4'b0010; #5;
b =4'b0011; #5;
b =4'b0100; #5;
b =4'b0101; #5;
b =4'b0110; #5;
b =4'b0111; #5;
```

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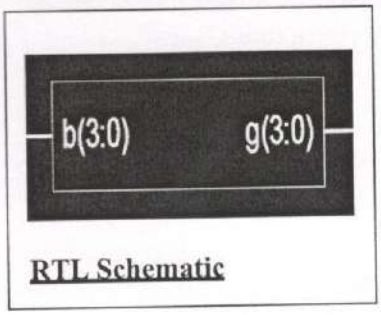


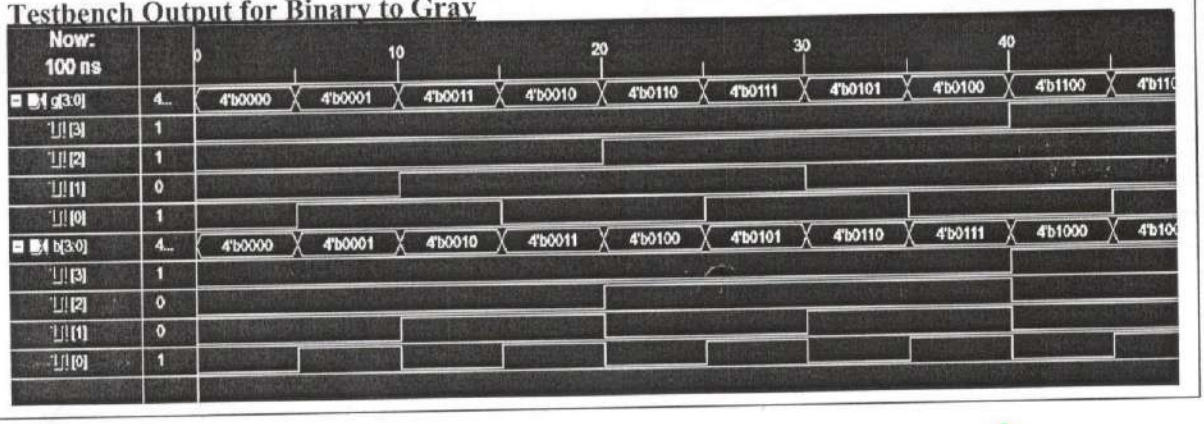
RTL Schematic

```
b =4'b1000; #5;
b =4'b1001; #5;
b =4'b1010; #5;
b =4'b1011; #5;
b =4'b1100; #5;
b =4'b1101; #5;
b =4'b1110; #5;
b =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs			
b3	b2	b1	b0	g3	g2	g1	g0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Testbench Output for Binary to Gray



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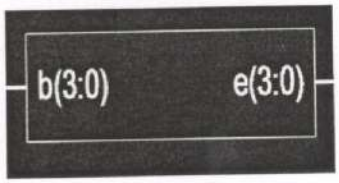
Top Module Code for Binary to Excess3

```
module binary_to_excess3 (b,e);
input [3:0] b;
output [3:0] e;
assign e = (b==0) ? 3: (b==1) ? 4: (b==2)
? 5: (b==3) ? 6: (b==4) ? 7: (b==5) ? 8:
(b==6) ? 9: (b==7) ? 10: (b==8) ? 11:
(b==9) ? 12: (b==10) ? 13 : (b==11) ? 14:
(b==12) ? 15: 4'bzzzz;
endmodule
```



RTL Schematic

Testbench Code for Binary to Excess3

```
module binary_to_excess3_test;
reg [3:0] b;
wire [3:0] e;
binary_to_excess3 uut(.b(b), .e(e));
initial
begin
b =4'b0000; #5;
b =4'b0001; #5;
b =4'b0010; #5;
b =4'b0011; #5;
b =4'b0100; #5;
b =4'b0101; #5;
b =4'b0110; #5;
b =4'b0111; #5;
b =4'b1000; #5;
b =4'b1001; #5;
b =4'b1010; #5;
b =4'b1011; #5;
b =4'b1100; #5;
b =4'b1101; #5;
b =4'b1110; #5;
b =4'b1111; #5;end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs			
b3	b2	b1	b0	e3	e2	e1	e0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	z	z	z	z
1	1	1	0	z	z	z	z
1	1	1	1	z	z	z	z

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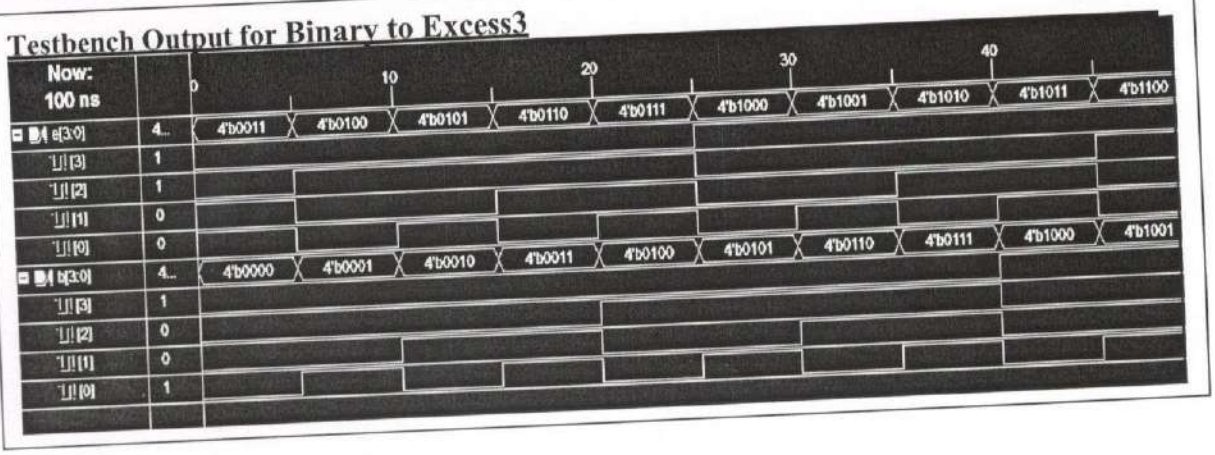
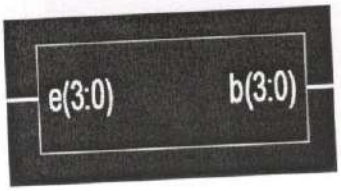
Testbench Output for Binary to Excess3



Top Module Code for Excess3 to Binary

```
module excess3_to_binary (e, b);
input [3:0] e;
output [3:0] b;
assign b  = (e==3) ? 0: (e==4) ? 1: (e==5)
? 2: (e==6) ? 3: (e==7) ? 4: (e==8) ? 5:
(e==9) ? 6: (e==10) ? 7 : (e==11) ? 8:
(e==12) ? 9: 4'bzzzz;
endmodule
```



RTL Schematic

Testbench Code for Excess3 to Binary

```
module excess3_to_binary_test;
reg [3:0] e;
wire [3:0] b;
excess3_to_binary uut(.b(b), .e(e));
initial
begin
e =4'b0000; #5;
e =4'b0001; #5;
e =4'b0010; #5;
e =4'b0011; #5;
e =4'b0100; #5;
e =4'b0101; #5;
e =4'b0110; #5;
e =4'b0111; #5;
e =4'b1000; #5;
e =4'b1001; #5;
e =4'b1010; #5;
e =4'b1011; #5;
e =4'b1100; #5;
e =4'b1101; #5;
e =4'b1110; #5;
e =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

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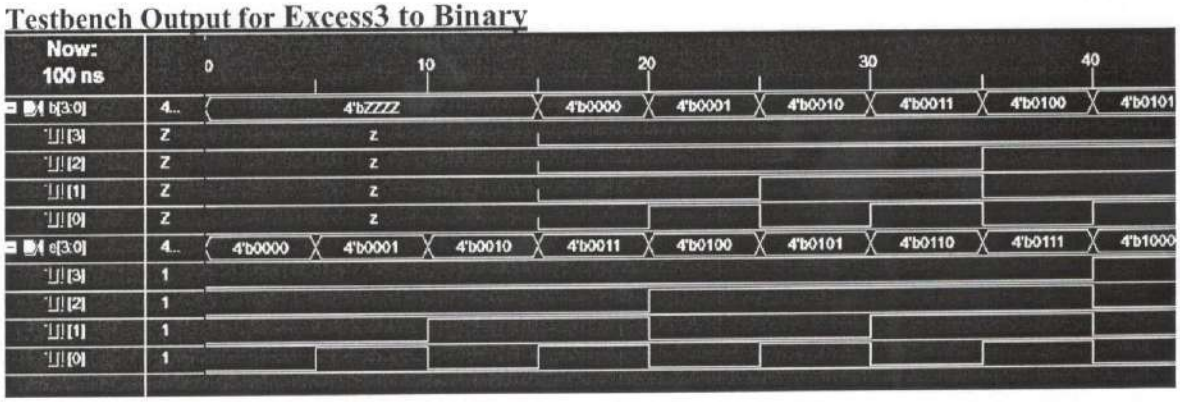
Truth Table

Inputs				Outputs			
e3	e2	e1	e0	b3	b2	b1	b0
0	0	0	0	z	z	z	z
0	0	0	1	z	z	z	z
0	0	1	0	z	z	z	z
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

Testbench Output for Excess3 to Binary



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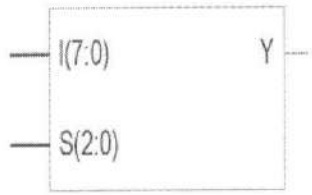
Experiment No: 5

AIM: To realize using Verilog Behavioral description: 8:1mux, 8:3encoder, Priority encoder

Top Module Code for 8:1 MUX

```
module 8_1_mux(Y, I, S);
output Y;
input [7:0] I;
input [2:0] S;
always@ (S, I)
begin
if (S==3'b000)
Y=I[0];
else if (S==3'b001)
Y=I[1];
else if (S==3'b010)
Y=I[2];
else if (S==3'b011)
Y=I[3];
else if (S==3'b100)
Y=I[4];
else if (S==3'b101)
Y=I[5];
else if (S==3'b110)
Y=I[6];
else if (S==3'b111)
Y=I[7];
else Y=1'bZ;
end
endmodule
```

RTL Schematic



Testbench Code for 8:1 MUX

```
module 8_1_mux_test;
reg [7:0] I;
reg [2:0] S;
wire Y;
8_1_mux uut(.I(I), .S(S), .Y(Y));
initial
begin
S=3'b000; I=8'b10010001; #10;
S=3'b001; #10;
S=3'b010; #10;
S=3'b011; #10;
S=3'b100; #10;
S=3'b101; #10;
S=3'b110; #10;
S=3'b111; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Output
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

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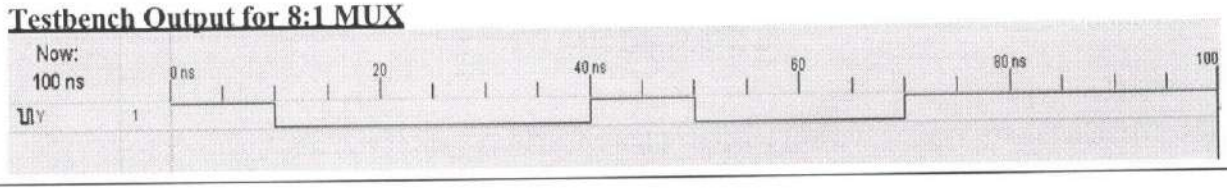
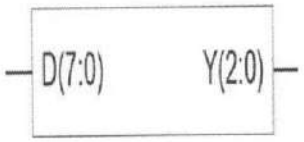
Testbench Output for 8:1 MUX



Top Module Code for 8:3 Encoder

```
module 8_3_encoder(Y, D);
input [7:0]D;
output [2:0]Y;
reg [2:0] Y;
always@ (D)
begin
case(D)
8'b00000001: Y=3'b000;
8'b00000010: Y=3'b001;
8'b00000100: Y=3'b010;
8'b00001000: Y=3'b011;
8'b00010000: Y=3'b100;
8'b00100000: Y=3'b101;
8'b01000000: Y=3'b110;
8'b10000000: Y=3'b111;
endcase
end
endmodule
```

RTL Schematic



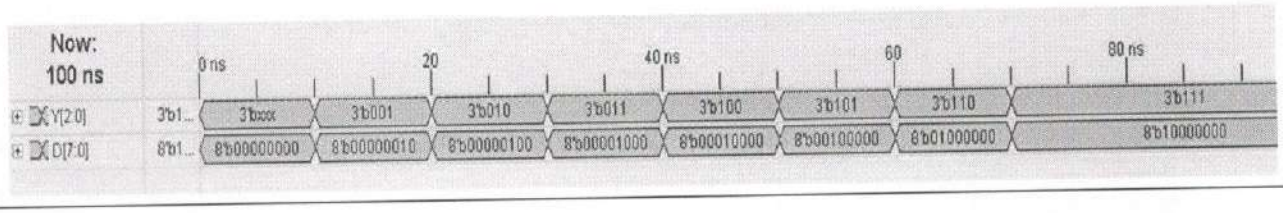
Testbench Code for 8:3 Encoder

```
module 8_3_encoder_test;
reg [7:0] D;
wire [2:0] Y;
8_3_encoder uut(.D(D),.Y(Y));
initial
begin
D=8'b00000000; #10;
D=8'b00000010; #10;
D=8'b00000100; #10;
D=8'b00001000; #10;
D=8'b00010000; #10;
D=8'b00100000; #10;
D=8'b01000000; #10;
D=8'b10000000; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs								Outputs		
D7	D6	D5	D4	D3	D2	D1	D0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

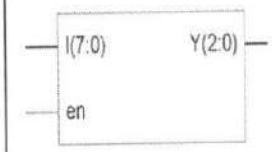
Testbench Output for 8:3 Encoder



Top Module Code for Priority Encoder

```
module 8_3_priorityencoder(Y, I, en);
output [2:0] Y;
input [7:0] I;
input en;
reg [2:0] Y;
always@ (en, I)
begin
if (en==1)
begin
if (I[7]==1) Y=3'b111;
else if (I[6]==1) Y=3'b110;
else if (I[5]==1) Y=3'b101;
else if (I[4]==1) Y=3'b100;
else if (I[3]==1) Y=3'b011;
else if (I[2]==1) Y=3'b010;
else if (I[1]==1) Y=3'b001;
else
Y=3'b000;
end
else Y=3'bzzz;
end
endmodule
```

RTL Schematic



Testbench Code for Priority Encoder

```
module 8_3_priorityencoder_test;
reg [7:0] I;
reg en;
wire [2:0] Y;
8_3_priorityencoder uut (.en(en), .I(I),
.Y(Y));
initial
begin
en=1;I=8'b1XXXXXXX; #10;
I=8'b01XXXXXX; #10;
I=8'b001XXXXX; #10;
I=8'b0001XXXX; #10;
I=8'b00001XXX; #10;
I=8'b000001XX; #10;
I=8'b0000001X; #10;
I=8'b00000001; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs								Outputs		
I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

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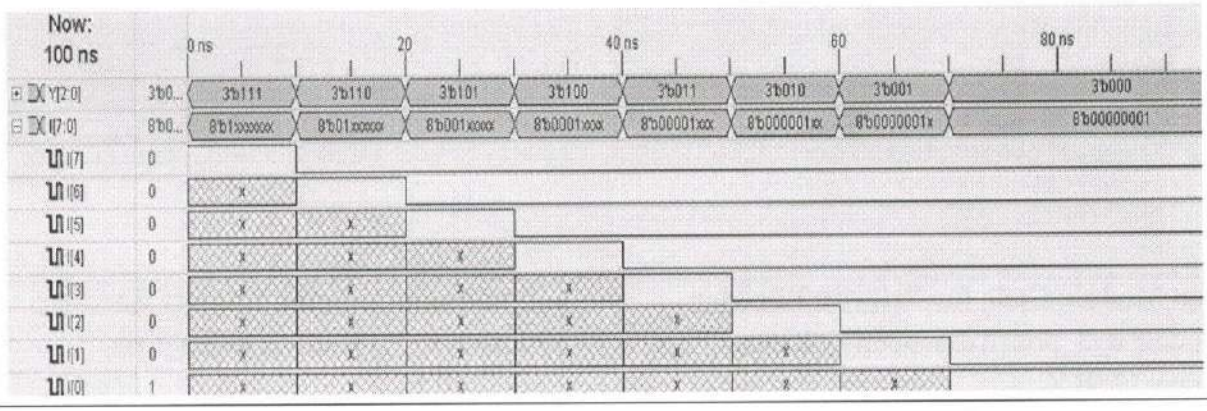
Testbench Output for Priority Encoder



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Experiment No: 6

AIM: To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder, 2 –bit Comparator

Top Module Code for 1:8 Demux

```
module 1_8_demux (i, s2, s1, s0, y);
output [7:0] y;
input i, s2, s1, s0;
reg [7:0] y;
always@ (i or s2 or s1 or s0)
begin
case ({s2, s1, s0})
0: y[0]=i;
1: y[1]=i;
2: y[2]=i;
3: y[3]=i;
4: y[4]=i;
5: y[5]=i;
6: y[6]=i;
7: y[7]=i;
endcase
end
endmodule
```

Testbench Code for 1:8 Demux

```
module 1_8_demux_test;
reg i, s2, s1, s0;
wire [7:0] y;
1_8_demux uut(.i(i),.s2(s2), .s1(s1), .s0(s0),
.y(y));
initial
begin
i=0; #10;
i=1; s2=0; s1=0; s0=0; #10;
s2=0; s1=0; s0=1; #10;
s2=0; s1=1; s0=0; #10;
s2=0; s1=1; s0=1; #10;
s2=1; s1=0; s0=0; #10;
s2=1; s1=0; s0=1; #10;
s2=1; s1=0; s0=0; #10;
s2=1; s1=1; s0=1; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Outputs							
S2	**S1**	**S0**	**Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**
0	0	0	0	0	0	0	0	0	0	i
0	0	1	0	0	0	0	0	0	i	0
0	1	0	0	0	0	0	0	i	0	0
0	1	1	0	0	0	0	i	0	0	0
1	0	0	0	0	0	i	0	0	0	0
1	0	1	0	0	i	0	0	0	0	0
1	1	0	0	i	0	0	0	0	0	0
1	1	1	i	0	0	0	0	0	0	0

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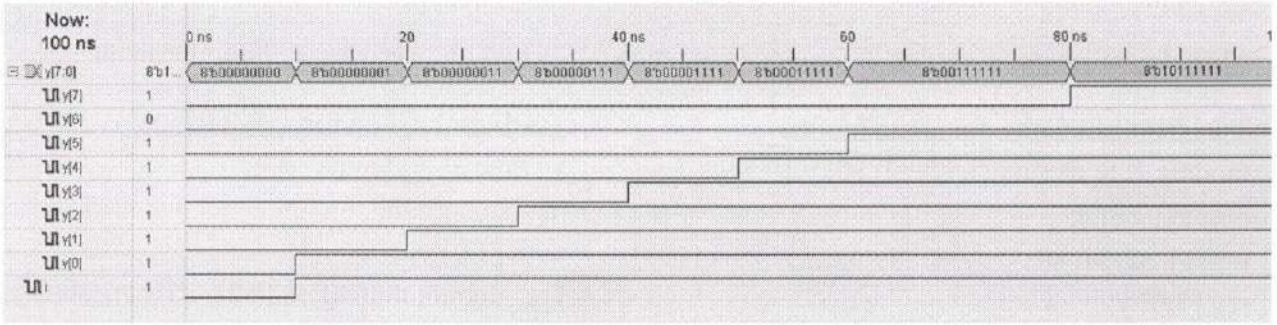
Testbench Output for 1:8 Demux



Top Module Code for 3:8 Decoder

```
module 3_8_decoder(Y, D);
output [7:0] Y;
input [2:0] D;
reg [7:0] Y;
always@ (D)
begin
case(D)
case(D)
3'b000: Y =8'b00000001;
3'b001: Y =8'b00000010;
3'b010: Y =8'b00000100;
3'b011: Y =8'b00001000;
3'b100: Y =8'b00010000;
3'b101: Y =8'b00100000;
3'b110: Y =8'b01000000;
3'b111: Y =8'b10000000;
endcase
end
endmodule
```

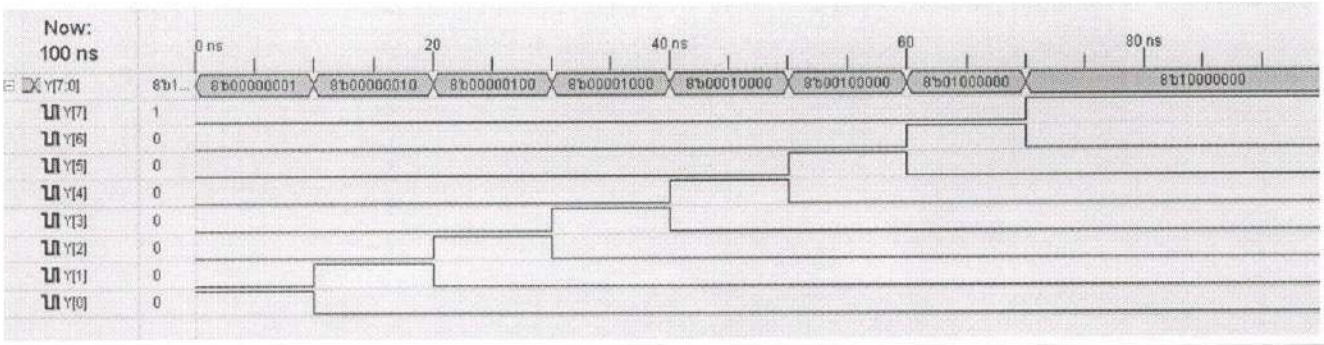
Testbench Code for 3:8 Decoder

```
module 3_8_decoder_test;
reg [2:0] D;
wire [7:0] Y;
3_8_decoder uut(.D(D),.Y(Y));
initial
begin
D=3'b000; #10;
D=3'b001; #10;
D=3'b010; #10;
D=3'b011; #10;
D=3'b100; #10;
D=3'b101; #10;
D=3'b110; #10;
D=3'b111; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Outputs							
D2	D1	D0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Testbench Output for 3:8 Decoder



Top Module Code for 2-bit comparator

```
module comp_2(a, b, greater, lesser, equal);
output greater, lesser, equal;
input [1:0] a,b;
reg greater, lesser, equal;
always@ (a or b)
begin
if (a > b)
begin
greater=1; lesser=0; equal=0;
end
else if (a < b)
begin
greater=0; lesser=1; equal=0;
end
else
begin
greater=0; lesser=0; equal=1;
end
end
endmodule
```

Testbench Code for 2-bit comparator

```
module comp_2_test;
reg [1:0] a,b;
wire greater, lesser, equal;
comp_2 uut(.a(a), .b(b), .greater(greater), .
lesser(lesser), .equal(equal));
initial
begin
a=0; b=0; #100;
a=5; b=2; #100;
a=2; b=5; #100;
a=5; b=5; #100;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs		
a1	**a0**	**b1**	**b0**	**a > b**	**a < b**	**a = b**
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0

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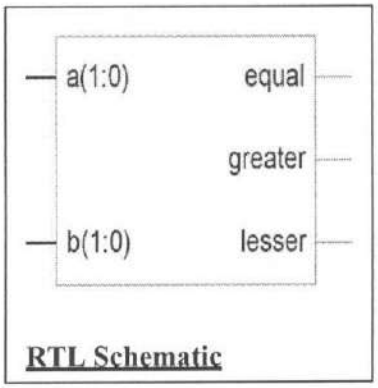
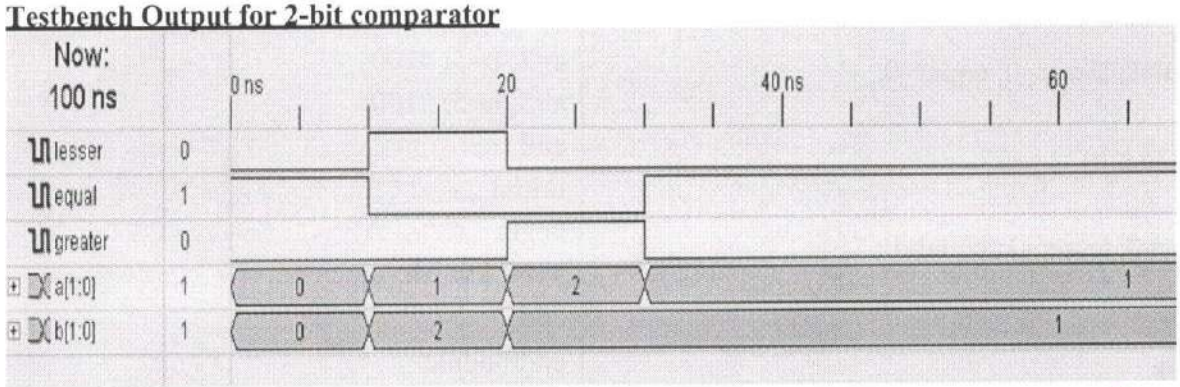
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0



RTL Schematic

Testbench Output for 2-bit comparator



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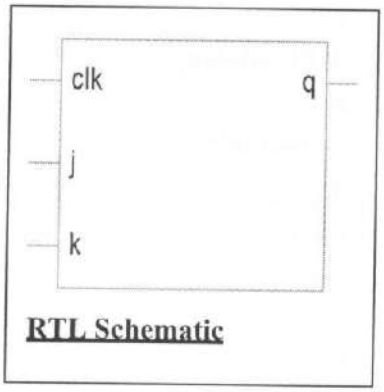
Experiment No: 7

AIM: To realize using Verilog Behavioral description:

Flip-flops: a)JK type b)SR type c)T type and d)D type

Top Module Code for JK Flip Flop

```
module jk_ff (j, k, clk, q);
output q;
input j, k, clk;
reg q;
always@ (posedge clk)
case ({j,k})
2'b00: q<=q;
2'b01: q<=0;
2'b10: q<=1;
2'b11: q<=~q;
endcase
endmodule
```



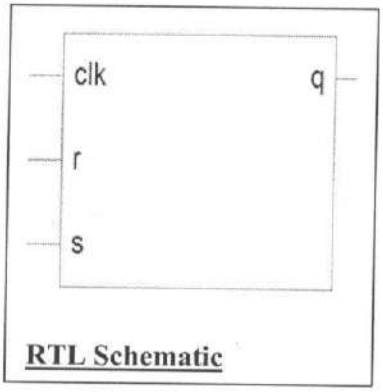
RTL Schematic

Testbench Code for JK Flip Flop

```
module jk_ff_test;
reg j,k,clk;
wire q;
jk_ff uut(.j(j), .k(k), .clk(clk), .q(q));
initial
begin
clk=0;
j=0; k=0; #10;
j=0; k=1; #10;
j=1; k=0; #20;
j=1; k=1; #5;
end
always #5 clk=~clk;
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for SR Flip Flop

```
module sr_ff (s, r, clk, q);
output q;
input s, r, clk;
reg q;
always@ (posedge clk)
case ({s,r})
2'b00: q<=q;
2'b01: q<=0;
2'b10: q<=1;
2'b11: q<=z;
endcase
endmodule
```



RTL Schematic

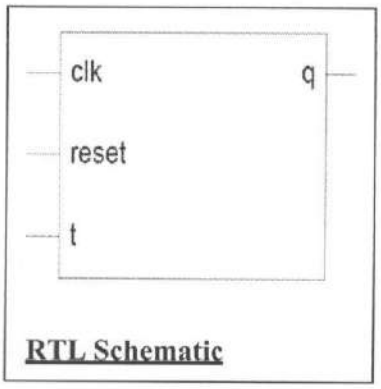
Testbench Code for SR Flip Flop

```
module sr_ff_test;
reg s,r,clk;
wire q;
sr_ff uut(.s(s), .r(r), .clk(clk), .q(q));
initial
begin
clk=0;
s=0; r=0; #10;
s=0; r=1; #10;
s=1; r=0; #20;
s=1; r=1; #5;
end
always #5 clk=~clk;
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for T Flip Flop

Testbench Code for T Flip Flop

```
module t_ff (t, reset, clk, q);
output q;
input t, reset, clk;
reg q;
always@ (posedge clk)
begin
if (reset)
q<=0;
else
if (t)
q <= ~q;
else
q <= q;
end
endmodule
```

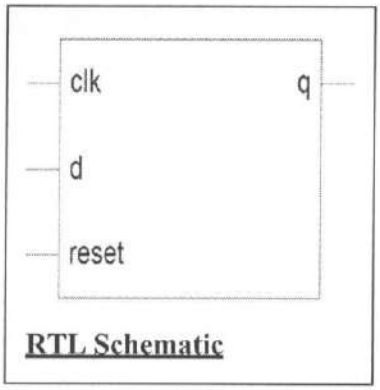


RTL Schematic

```
module t_ff_test;
reg t,reset,clk;
wire q;
t_ff uut(.t(t), .reset(reset), .clk(clk),  .q(q));
always #5 clk = ~clk;
initial
begin
clk=0;
t = 0;
reset = 1;
#10;
t=0; reset=0; #10;
t=1; #100;
end
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for D Flip Flop

```
module d_ff (d, reset, clk, q);
output q;
input d, reset, clk;
reg q;
always@ (posedge clk)
begin
if (reset)
q<=0;
else
q <= d;
end
endmodule
```



RTL Schematic

Testbench Code for D Flip Flop

```
module d_ff_test;
reg d;
reg reset;
reg clk;
wire q;
d_ff uut (.d(d), .reset(reset), .clk(clk),
.q(q));
initial begin
clk=0;
d = 0;
reset = 1;
#100;
d = 0;
reset = 0;
#100;
d = 1;
end
always #5 clk=~clk;
endmodule
```

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Truth Table for J K Flip Flop

clk	J	K	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	~q --Toggle

Truth Table for SR Flip Flop

clk	S	R	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	X --Indeterminate

Truth Table for T Flip Flop

clk	reset	T	q
↑	0	0	q --No change
↑	0	1	~q --Toggle
↑	1	0	0 --Reset
↑	1	1	0 --Reset

Truth Table for D Flip Flop

clk	reset	D	q
↑	0	0	D -- Input
↑	0	1	D --Input
↑	1	0	0 --Reset
↑	1	1	0 --Reset

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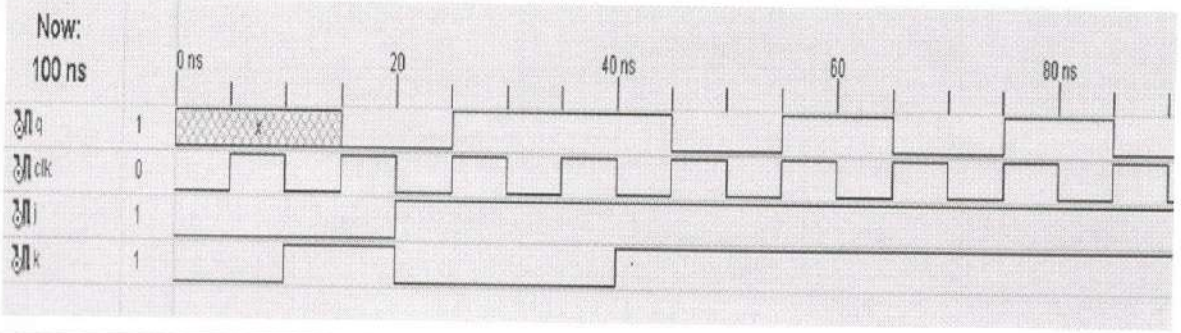
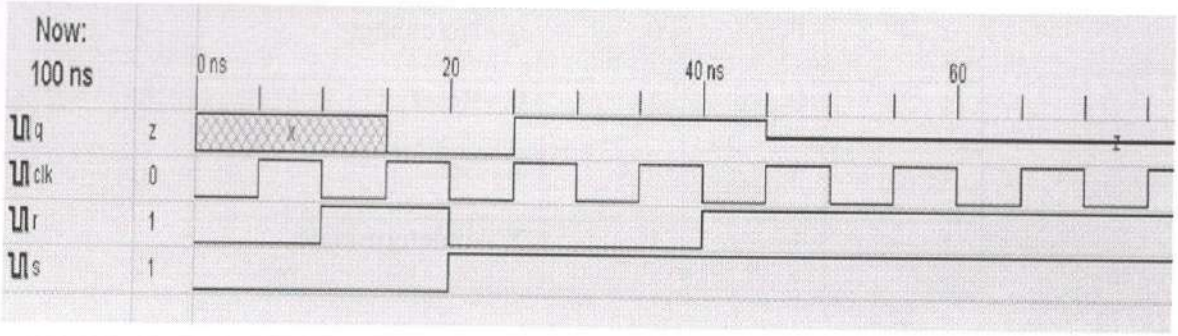
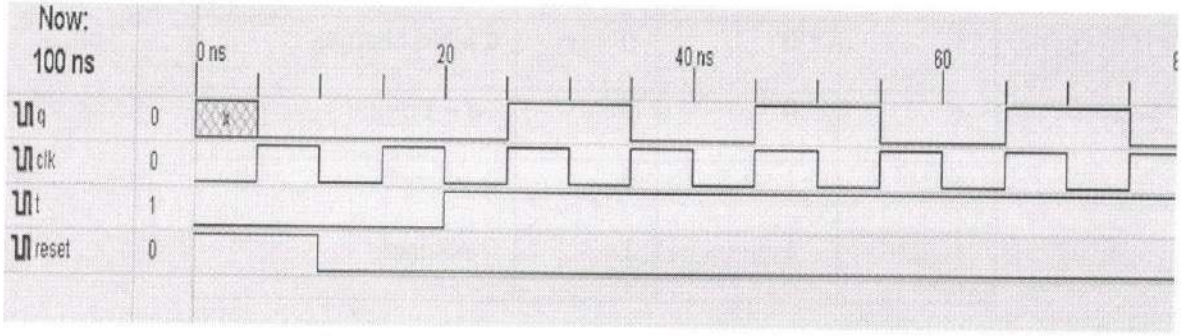
Testbench Output for JK Flip Flop



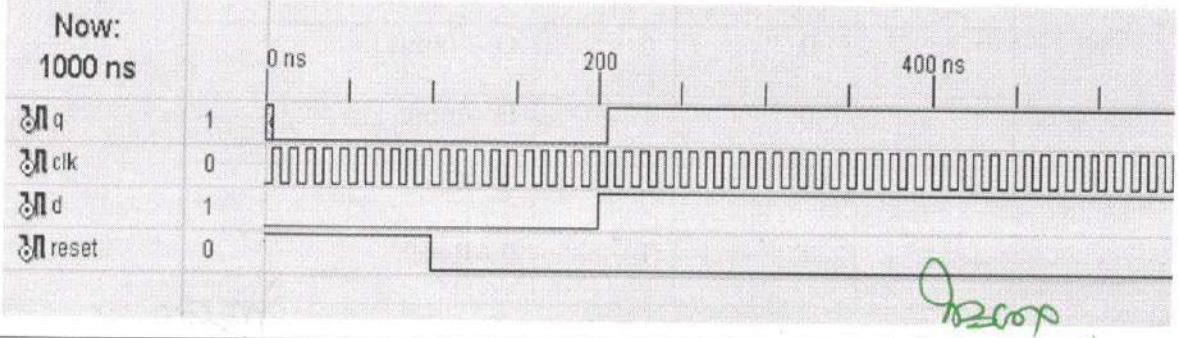
Testbench Output for SR Flip Flop



Testbench Output for T Flip Flop



Testbench Output for D Flip Flop



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Truth Table for J K Flip Flop

clk	J	K	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	~q --Toggle

Truth Table for SR Flip Flop

clk	S	R	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	X --Indeterminate

Truth Table for T Flip Flop

clk	reset	T	q
↑	0	0	q --No change
↑	0	1	~q --Toggle
↑	1	0	0 --Reset
↑	1	1	0 --Reset

Truth Table for D Flip Flop

clk	reset	D	q
↑	0	0	D -- Input
↑	0	1	D --Input
↑	1	0	0 --Reset
↑	1	1	0 --Reset

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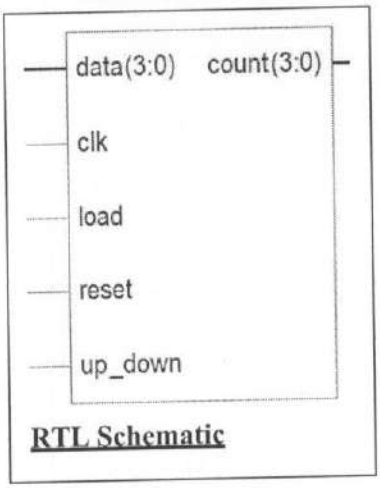
Experiment No: 8

AIM: To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.

Top Module Code for 4-bit Binary Up/Down Counter

```
module binary_counter
(clk,reset,up_down,load,data,count);
input clk,reset,load,up_down;
input [3:0] data;
output [3:0] count;
reg [3:0] count;
always@(posedge clk)
begin
if(reset)
count <= 0;
else if(load)
count <= data;
else if(up_down)
count <= count + 1;
else
count <= count - 1;
end
endmodule
```



RTL Schematic

Testbench Code for 4-bit Binary Up/Down Counter

```
module binary_counter_test;
reg clk;
reg reset;
reg up_down;
reg load;
reg [3:0] data;
wire [3:0] count;
binary_counter uut (.clk(clk), .reset(reset),
.up_down(up_down), .load(load),
.data(data), .count(count));
initial begin clk = 1'b0;
repeat(30)
#3 clk= ~clk;
end
initial begin reset=1'b1;
#7 reset=1'b0;
#35 reset=1'b1;
end
initial begin
#12 load=1'b1;
#5 load=1'b0;
end
initial begin
#5 up_down=1'b1;
#24 up_down=1'b0;
end
initial begin
data=4'b1000;
#14 data=4'b1101;
#2 data=4'b1111;
end
endmodule
```

Top Module Code for 4-bit BCD Up/Down Counter

```
module bcd_counter (clk, reset, count);
input clk, reset;
output [3:0] count;
reg [3:0] count;
```

Testbench Code for 4-bit BCD Up/Down Counter

```
module bcd_counter_tb;
reg clk, reset;
wire [3:0] count;
wire [3:0] tmp;
```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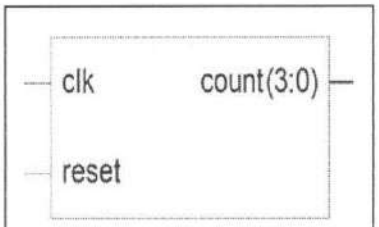
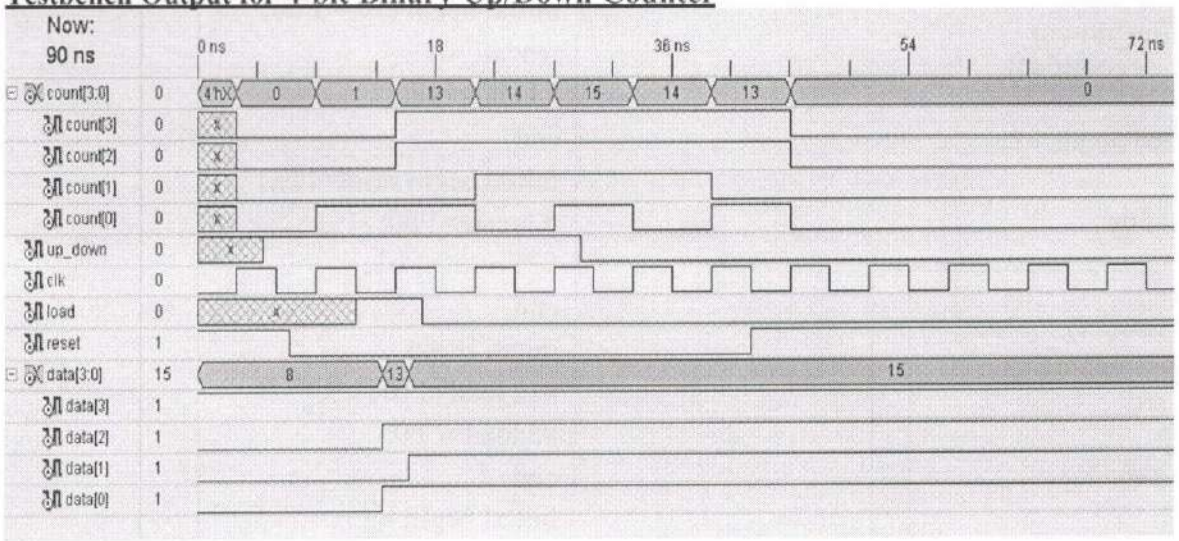
```
reg [3:0] tmp;
always@(posedge clk)
begin
if(reset)
begin
count <= 4'b0000;
tmp <= 4'b0000;
end
else
begin
tmp <= tmp + 1;
if (tmp==4'b1001)
begin
tmp <= 4'b0000;
end
count <= tmp;
end
end
endmodule
```



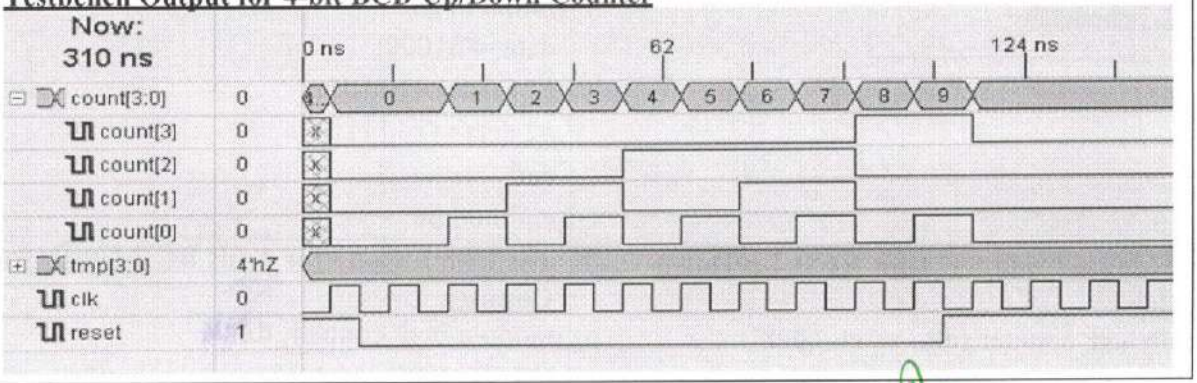
RTL Schematic

```
bcd_counter uut(.clk(clk), .reset(reset),
.count(count));
initial begin
clk = 0;
forever #5 clk = ~ clk;
end
initial begin
reset =1;
#10 reset =0;
#100 reset =1;
#200;
$finish;
end
endmodule
```

Testbench Output for 4-bit Binary Up/Down Counter



Testbench Output for 4-bit BCD Up/Down Counter



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Demonstration Experiments

Experiment No: 1

AIM: Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).

```
module stepper(clk,dir,reset,dout);
input clk, dir, reset;
output [3:0] dout;
reg [3:0] dout;
reg [3:0] shift;
always@ (posedge clk)
begin
clk_div= clk_div+1;
currentstate=nextstate;
end
always@ (posedge clk_div[15])
begin
if (reset==0)
shift=4'b0001;
else if (dir==1)
shift={shift[0], shift[3:1]};
else
shift={shift[2:0], shift[3]};
dout=shift;
end
endmodule
```

UCF File

```
NET "clk" LOC = "p52"
NET "dir" LOC = "p74"
NET "reset" LOC = "p76"
NET "dout<0>" LOC = "p84"
NET "dout<1>" LOC = "p85"
NET "dout<2>" LOC = "p86"
NET "dout<3>" LOC = "p87"
```

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Experiment No: 2

AIM: Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

```
module led_switch (led, switch);
output led;
input switch;
assign led=switch;
endmodule
```

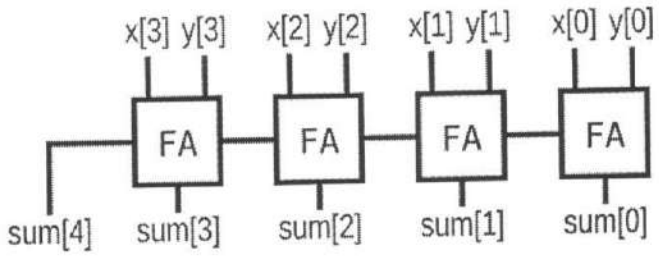
CONTENT BEYOND SYLLABUS

1. Consider the function *f* shown in the Karnaugh map below. Implement this function. **d** is don't-care, which means you may choose to output whatever value is convenient.

x_3x_4 \ x_1x_2	00	01	11	10
00	d	0	d	d
01	0	d	1	0
11	1	1	d	d
10	1	1	0	d

2. Suppose you are designing a circuit to control a cellphone's ringer and vibration motor. Whenever the phone needs to ring from an incoming call (`input` **`ring`**), your circuit must either turn on the ringer (`output` **`ringer`** `= 1`) or the motor (`output` **`motor`** `= 1`), but not both. If the phone is in vibrate mode (`input` **`vibrate_mode`** `= 1`), turn on the motor. Otherwise, turn on the ringer. Try to use only `assign` statements, to see whether you can translate a problem description into a collection of logic gates.

3. Implement the following circuit:



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BANTAKAL - 574 115

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A Unit of Shri Sode Vadiraja Mutt Education Trust (R), Udupi
(Affiliated to Visvesvaraya Technological University, Belagavi)

Vishwothama Nagar, BANTAKAL - 574 115
Udupi District, Karnataka, INDIA

SMVITM

RECORD BOOK

Name NISHA USN 4MW22EC049

Semester 3rd Year 2023-24

Lab Name DSD using verilog Section A

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Udupi District, Karnataka, INDIA

SMVITM

DEPARTMENT OF Electronics and Communication.

Certificate

This is to certify that ~~Mr.~~ / Ms. Nisha

bearing USN 4MW22EC079 has satisfactorily completed the laboratory course Digital System design using verilog lab prescribed by the Visvesvaraya Technological University, Belagavi for the 3rd semester of Bachelor of Engineering in electronics and communication Engineering during the year 2023-24.

27/02/2024

Faculty In-charge

Head of the Department
Dept of E&C Engg.
SMVITM, BANTAKAL - 574 115

19
25

Marks awarded

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INSTITUTE VISION

"To Establish an Excellent, Value-based Higher Educational Hub to Meet the Challenges of Global Competitiveness"

INSTITUTE MISSION

"To impart holistic education with state of the art infrastructural facilities and conducive academic ambience, at affordable costs, leading to the creation of Centers of Excellence with best brains collectively interacting for total personality development and intellectual growth."

DEPARTMENT VISION

To be recognized as a center of eminence in the field of Electronics and Communication Engineering for holistic engineering education and research on current technologies.

DEPARTMENT MISSION

1. Impart quality engineering education with ethics to students and transform them into leaders in technology, innovation and research.
2. Provide a platform and academic atmosphere that will ensure the transfer of knowledge and skills to the students.
3. Promote the overall personality development of the students through activities that have high credibility and social impact.

PROGRAM EDUCATIONAL OBJECTIVES

The graduate of Electronics and Communication Engineering should be able to

PEO-1 Exhibit essential knowledge of applied sciences mathematical modelling, logical interpretation and visual realization to resolve real-time problems in the field of electronics and communication engineering.

PEO-2 Work productivity as an electronics and communication engineer, including supportive and leadership roles on multidisciplinary teams.

PEO-3 Inculcate effective communication skills to excel in professional growth.

PEO-4 Take part in lifelong learning in pace with the advancing technological society.

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EVALUATION SCHEME

Sl. No.	Description	Marks	
		Maximum	Alloted
1.	Continuous Internal Evaluation	15	15
2	Internal Assessment	10	04
	TOTAL	25	19

Student Signature

07/02/2024

Faculty Signature

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COURSE OUTCOMES

This course will enable the students to:

- To impart the concepts of simplifying the Boolean expression using k-map techniques and Quine-Mc cluskey minimization techniques.
- To impart the concepts of designing and analysing combinational logic circuits.
- To impart design methods and analysis of sequencing logic circuits.
- To impart the concepts of Verilog-HDL dataflow and behavioural models for the design of digital systems.

PROGRAM OUTCOMES

PO 1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2 **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4 **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6 **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7 **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10 **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

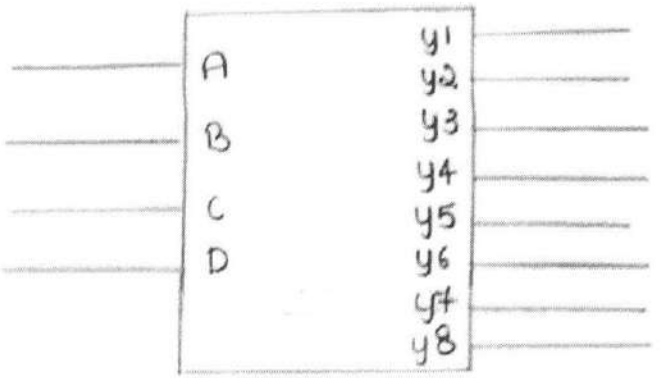
PO 12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

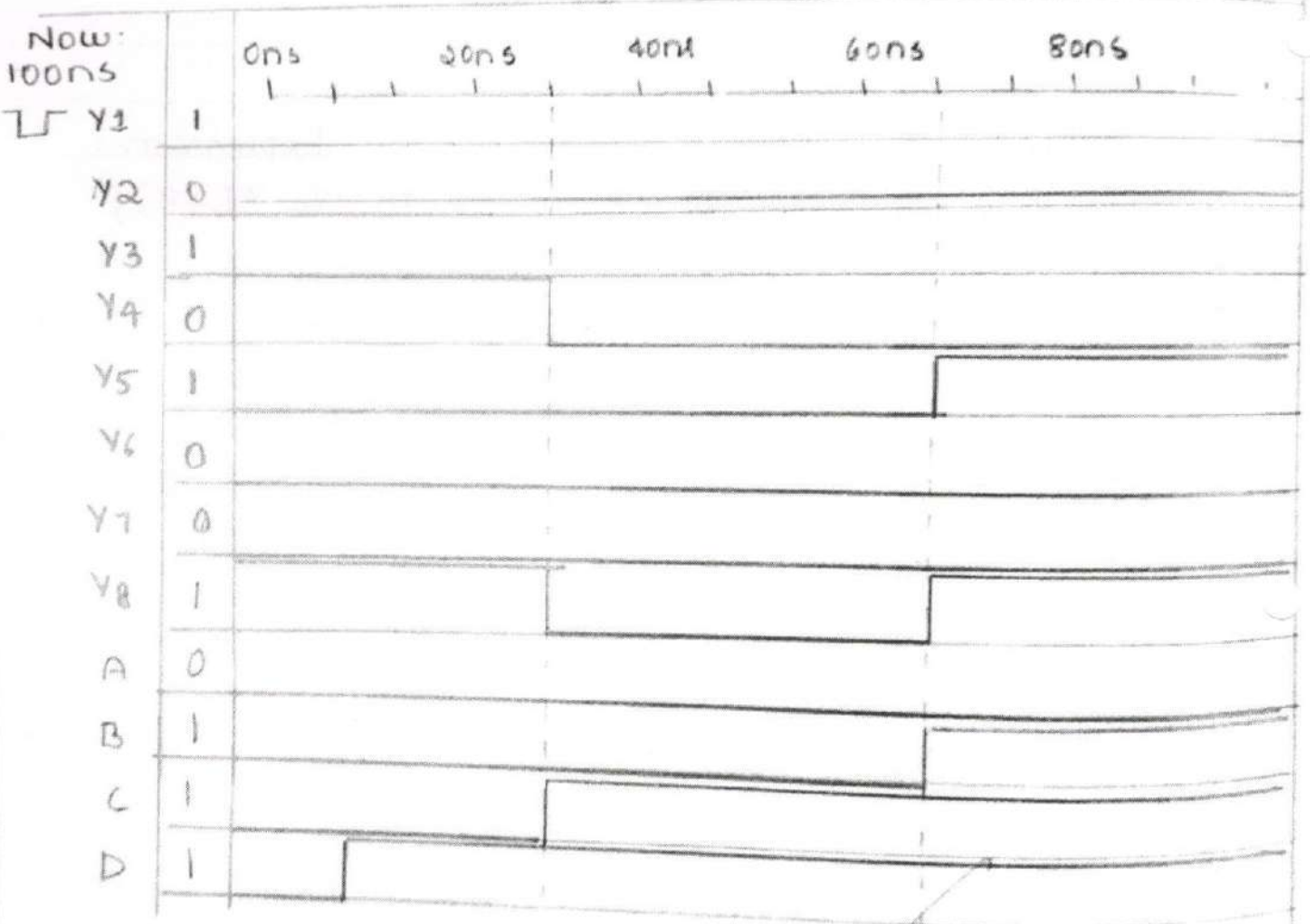
PSO1: Understand the concepts of electronics and communication engineering and its applications in the fields of signal processing, control system, VLSI design, networking and communication.

PSO2: Apply the domain specific knowledge to design, analyse, synthesize and validate real time problems in electronics and communication engineering.

RTL Schematic



Testbench output:



$Y1 = A'B' + AB + A'B$.

$= A'(B'+B) + AB$

$= A' + AB$

$= A' \cdot 1 + AB$

$= A' + B(A'+A)$

$= A' + B(A'+A) = A' + B$ //.

$Y2 = (A+B)(A+B')$

$= AA + AB' + AB + BB'$

$= A + A(B'+B)$

$= A + A(1)$

$= A$

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Experiment No. 1

Date 20/11/23

Aim: To simplify the given Boolean expressions and realize using Verilog program.

$Y1 = A'B' + AB + A'B$.

$Y2 = (A+B)(A+B')$

$Y3 = A'B + AB' + A'B' + AB$

$Y4 = AB' + BC' + AC'$

$Y5 = A'BC + AC$

$Y6 = AB + ACCD + CD')$

$Y7 = (BC' + A'D)(AB' + CD')$

$Y8 = A'BC + AB'C' + A'B'C' + ABC$

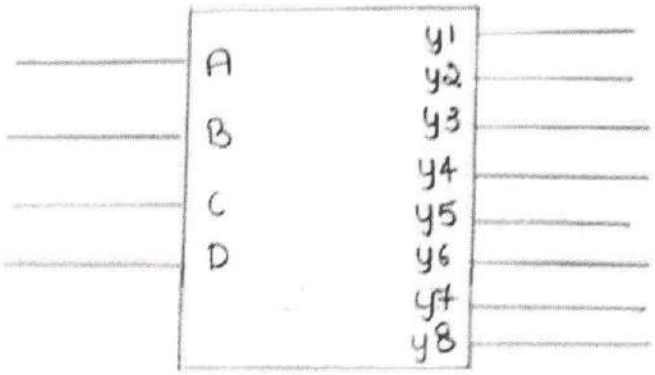
Top Module Program for Boolean Expression:

```
module bool(A,B,C,D,Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8);
input A,B,C,D;
output Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
assign Y1 = ~A|B;
assign Y2=A;
assign Y3=1;
assign Y4=(A&(~B))|((~A)&(~C));
assign Y5= C&(A|B);
assign Y6 = A&(B|C);
assign Y7=0;
assign Y8=(B&C)|((~B)&(~C));
endmodule
```

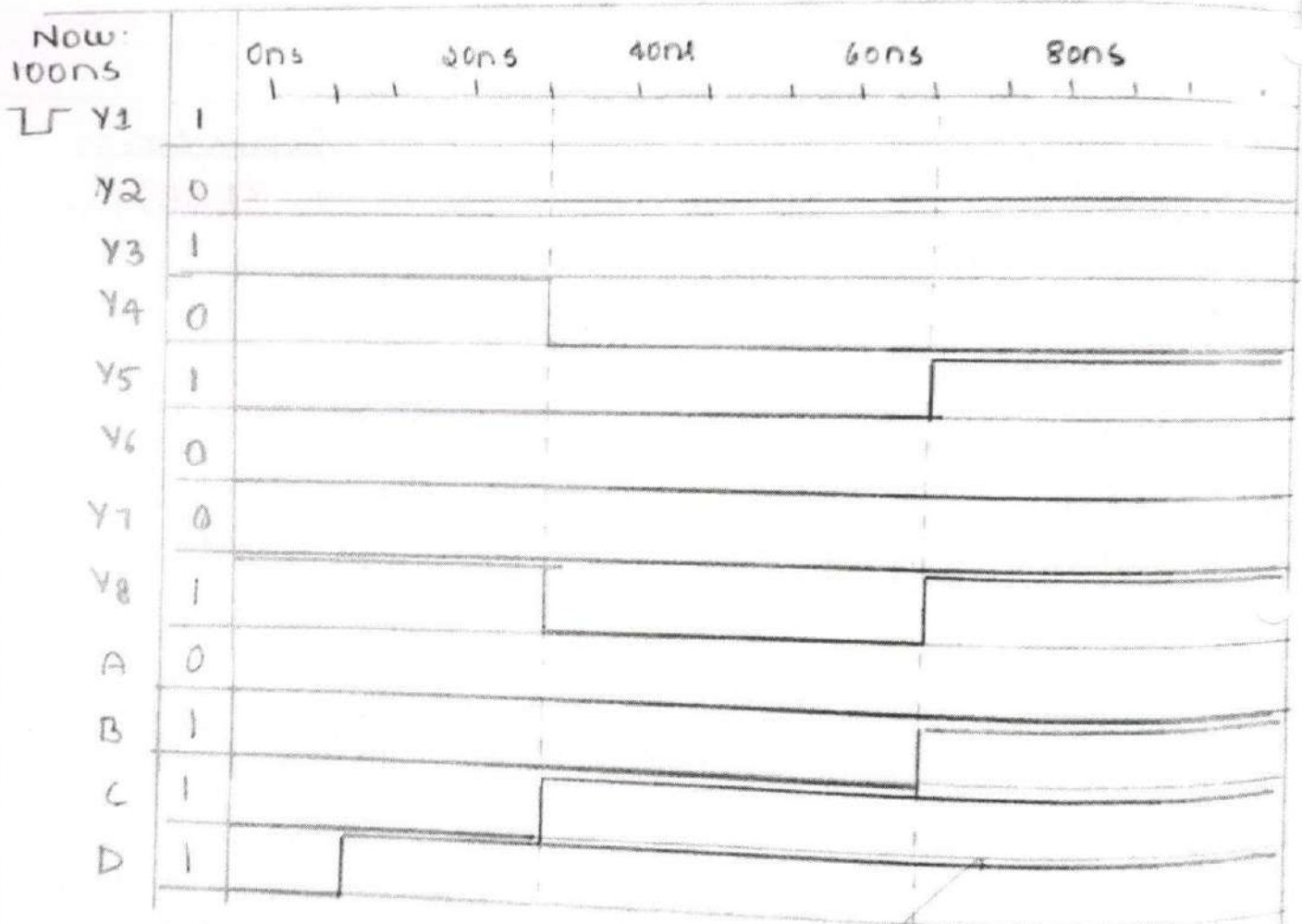
TestBench code for Boolean Expression

```
module bool_test;
reg A,B,C,D;
wire Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
```

RTL Schematic



Testbench output:



$Y1 = A'B' + AB + A'B$.

$= A'(B'+B) + AB$.

$= A' + AB$

$= A' \cdot 1 + AB$

$= A' + B(A'+A)$

$= A' + B(A'+A) = A' + B$ //.

$Y2 = (A+B)(A+B')$

$= AA + AB' + AB + BB'$

$= A + A(B'+B)$

$= A + A(1)$

$= A$

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Experiment No.

Date

```
bool uut (.A(A), .B(B), .C(C), .D(D), .Y1(Y1), .Y2(Y2), .Y3(Y3), .Y4
(Y4), .Y5(Y5), .Y6(Y6), .Y7(Y7), .Y8(Y8));
initial
begin
A=0; B=0; C=0; D=0;
end
always
begin
#10 D=!D;
#20 C=!C;
#40 B=!B;
#80 A=!A;
end
initial
begin
#200 $finish;
end
endmodule
```


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~~Truth Table~~ :

$Y3 = A'B + BB' + A'B' + AB$

$= A'(B+B') + A(B'+B)$

$= A'(1) + A(1) = A' + A$

$= \underline{1}$

$Y4 = AB' + B'C' + A'C'$

$= AB' + A'C' + B'C'(A+A')$

$= AB' + A'C' + AB'C' + A'BC'$

$= AB'(1+C') + A'C'(1+B') + A'B'C'$

$= AB'(1+C') + A'C'$

$= \underline{AB' + A'C'}$

$Y5 = A'BC + AC$

$= A'BC + AC(B+B')$

$= A'BC + ABC + AB'C$

$= BC(A'+A) + AB'C$

$= BC + AB'C$

$= C(B + AB')$

$= C(B+A) = \underline{BC + AC}$

$Y6 = AB + AC(D+CD')$

$= AB + ACD + ACD'$

$= AB + AC(D+D')$

$= AB + AC = \underline{A(B+C)}$

$Y7 = (BC' + A'D)(AB' + CD')$

$= BC' \cdot AB' + B'C' \cdot CD' + A'D \cdot AB' + A'D \cdot CD'$

$= 0$

$Y8 = A'BC + AB'C' + A'B'C' + ABC$

$= A'BC + B'C'(A+A') + ABC$

$= A'BC + B'C' + ABC$

$= BC(A'+A) + B'C'$

$Y8 = \underline{BC + B'C'}$

Truth Table :

Inputs				Outputs							
A	B	C	D	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	1	0	1	1	0	0	0	1
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	1	0	1	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	0
0	1	0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	1	0	1	0	1	0	0	1
0	1	1	1	0	1	1	0	1	0	0	1
1	0	0	0	1	0	1	1	0	0	0	1
1	0	0	1	0	1	1	1	0	0	0	1
1	0	1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	1	1	0	0	0	0	0
1	1	0	0	1	0	1	1	0	0	0	0
1	1	0	1	0	1	1	1	0	0	0	0
1	1	1	0	1	0	1	0	0	0	0	0
1	1	1	1	0	1	1	0	0	0	0	0