Dissemination of POs and PSOs

Programme Outcomes and Program Specific Outcomes are stated, displayed and disseminated to internal and external stakeholders through the following:

- College Website
- Course Files
- Department Entrance
- Department Notice Boards
- Program Assessment Committee Meeting
- Parent Teachers Meeting
- Orientation Program
- Event Brochures
- Department Newsletter

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COURSE FILE (2022-23)

Department: ELECTRONICS & COMMUNICATION ENGINEERING **Class: 7th Sem**

Course Title: Radar Engineering **Course code: 18EC823**

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1. Course details

1.1 Primary information

1	**Course Code**	18EC823
2	**L-T-P**	3-0-0
3	**Course Credit**	3
4	**Marks (Min/Max)** **VTU Exam** **Internal Assessment**	40/100 35/100 16/40
5	**Pre-requisite**	Analog and Digital Communication, Microwave and Antenna

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6	**Teaching Department**	Electronics & Communication Engineering
7	**Course Duration**	40 Hours
8	**Faculty Handling the course**	Mr. Arun Upadhyaya
9	**Course Coordinator**	Mr. Arun Upadhyaya

1.2 Textbooks

1. Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001.

1.3 Reference Books

1. Radar Principles, Technology, Applications — Byron Edde, Pearson Education,2004.
2. Radar Principles – Peebles. Jr, P.Z. Wiley. New York. 1998.
3. Principles of Modem Radar: Basic Principles – Mark A. Rkhards, James A. Scheer, William A. Holm. Yesdee, 2013.

1.4 Other Resources (Online, Text, Multimedia, etc.)

1. https://nptel.ac.in/courses/108/105/108105154/
2. https://ocw.mit.edu/resources/res-ll-001-introduction-to-radar-systems-spring-2007/

1.5 Link of class web page (Google classroom/CANVAS etc.)

https://classroom.google.com/c/NTk2MTk0MTI0ODE2
vtnv6gk

2. Course Plan

2.1 Course Outcomes

Sl. No.	At the end of the course, Students will be able to	Bloom's Level	Target Attainment
CO1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	L3	2.2
CO2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	L3	2.2
CO3	Explain the working and applications of different types of Radar.	L2	2.2
CO4	Describe the working of various radar antennas and receivers.	L2	2.2

Cognitive levels as per Bloom's Taxonomy: L1-Remembering, L2-Understanding, L3-Applying, L4-Analyzing, L5-Evaluating and L6-Creating

2.2 Mapping of COs with POs (Course articulation matrix)

	Engineering Knowledge	Problem Analysis	Design &Development of Solutions	Investigations of Complex	Usage of Modern Tools	Engineer & Society	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Management & Finance	Life-long Learning		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1							1	3			2	1
CO2	2	1											1	1
CO3	2	1											1	1
CO4	2								1	3			1	

POs Mapping Level: 1-Slightly 2-Moderately 3-Highly

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2.3 Justification for CO-PO mapping

		Justification	Performance Indicator
CO1	PO1	Apply the knowledge of mathematics and engineering fundamentals to derive the equation for radar range.	1.1.1, 1.1.2, 1.3.1, 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems using radar range equation.	2.1.1, 2.1.2, 2.1.3, 2.4.1
	PO9	Demonstrate effective communication skill to explain the concepts like origins of radar and its applications.	9.2.1
	PO10	Read, understand and interpret technical and non-technical information and Deliver effective oral presentations to technical and non-technical audiences by using Use a variety of media effectively to convey a message in a document or presentation to understand concepts like origins of radar and its applications.	10.1.1 10.1.3, 10.2.2, 10.3.1, 10.3.2
	PSO1	Understand the concepts of communication in the field of radar engineering.	--
	PSO2	Apply domain-specific knowledge to understand the use of radar in communication engineering.	--
CO2	PO1	Apply the knowledge of mathematics and engineering fundamentals to determine the impact of noise on radar range equation.	1.1.1, 1.3.1, 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems on modified radar range equation.	2.1.2, 2.1.3 2.2.4, 2.4.1
	PSO1	Apply the concepts of noise in radar communication.	--
	PSO2	Understand the problems related to impact of noise on radar communication.	--
CO3	PO1	Apply the knowledge of mathematics and engineering fundamentals to understand the working and applications of different types of Radar	1.1.1, 1.3.1 1.4.1
	PO2	Identify the mathematical, engineering and other relevant knowledge and apply to solve the problems on Doppler frequency and measurement of speed of targets.	2.1.2, 2.1.3 2.4.1
	PSO1	Understand the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets in radar communication.	--
	PSO2	Understand the problems on Doppler frequency used in radar communication.	--
CO4	PO1	Apply the knowledge of mathematics and engineering fundamentals to understand the working of various radar antennas and receivers.	1.3.1 1.4.1
	PO9	Demonstrate effective communication skill to explain the concepts like types of antennas and receivers.	9.2.1
	PO10	Read, understand and interpret technical and non-technical information and Deliver effective oral presentations to technical and non-technical audiences by using Use a variety of media effectively to convey a message in a document or presentation to understand concepts like types of antennas and receivers.	10.1.1 10.1.3, 10.2.2, 10.3.1, 10.3.2
	PSO1	Understand the use of types of antennas in radar communication systems	--

2.4 Continuous Improvement (Actions taken based on the comments/suggestions of the AY: 2020-21)

SI	Scope for Improvement/Comments/Curriculum Gap (2020-21)	Action Items
1	Most of the topics are covered through Online mode/ Few topics can be covered online mode and remaining through offline	Few topics are covered online mode
2	Need to take more hours to complete the portion	Extra classes taken

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2.5 Topic Level Outcomes

Module	Topic	Topic Level Outcomes (TLO) At the end of the topic, the students will be able to	Blooms Level (L1–L6)	Relevant CO	Assessment Tools
Module-1	**Basics of Radar:** Introduction, Maximum Unambiguous Range, Radar Waveforms, Definitions - PRF, PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. **Simple form of the Radar Equation,** Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar. Illustrative Problems.	**1.1** Understand the working principle of Radar system.	L2	CO1	Internal Assessment /Assignment
		1.2 Define parameters related to Radar system.	L1		
		1.3 Explain simple form of Radar equation.	L3		
		1.4 Explain applications of Radar system and origins of Radar.	L2		
Module-2	**The Radar Equation:** Prediction of Range Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector —Probability of Detection. **Radar Cross Section of Targets:** sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses. Illustrative Problems.	**2.1** Derive the modified equation or radar range with signal to noise ratio.	L2	CO2	Internal Assessment /Assignment
		2.2 Compute probability of detection and false alarm.	L3		
		2.3 Identify different Radar cross section of targets.	L2		
		2.4 Find out transmitter power, pulse repetition frequency and system losses.	L3		
Module-3	**MTI and Pulse Doppler Radar:** Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Delay Line Canceler, MTI Radar with – Power Amplifier Transmitter, Blind Speeds, Clutter Attenuation, MTI Improvement Factor, N- Pulse Delay-Line Canceler, **Digital MTI Processing** – Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector- Original MTD	**3.1** Understand the Principles of MTI and Pulse Doppler Frequency Shift Radars.	L2	CO2	Internal Assessment /Assignment
		3.2 Explain the purpose of delay line canceller and clutter attenuation and derive the frequency response of delay line canceller,	L2		
		3.3 Describe the working of Digital MTI Processing and moving target detectors.	L2		
Module-4	**Tracking Radar:** Tracking with Radar-Types of Tracking Radar Systems, Monopulse Tracking- Amplitude Comparison Monopulse (one-and two-coordinates), and Phase Comparison	**4.1** Understand the types of Tracking Radar Systems.	L2	CO3	Internal Assessment /Assignment
		4.2 Describe mono-pulse tracking.	L2		

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	Monopulse. **Sequential Lobing**, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range, Comparison of Trackers.	**4.3** Explain Conical Scan Tracking Radar.	L2		
Module-5	**The Radar Antenna:** Functions of The Radar Antenna, Antenna Parameters, Reflector Antennas and Electronically Steered Phased array Antennas. The Radar Receiver, Receiver Noise Figure, Super Heterodyne Receiver, Duplexers and Receivers Protectors, Radar Displays.	**5.1** Different functions served by Radar antenna and types of antennas used in radar.	L2	**CO4**	Internal Assessment /Assignment
		5.2 Understand the Radar receiver and role of duplexer's in Radar system.	L2		
		5.3 Explain different types of Radar display systems, receiver protectors	L2		

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2.6 Course Delivery Schedule

Lect. /Tut No.	Topics to be covered	Relevant TLO	Date on which topics covered	Mode of Delivery	Faculty Sign (Every class)	HoD Sign (Every Module)
	Module 1					
L1	Basics of Radar: Introduction, Maximum Unambiguous Range	1.1	17/2	BB		
L2	Radar Waveforms, Definitions with respect to pulse waveform - PRF, PRI,	1.2	17/2	BB		
L3	Definitions with respect to pulse waveform - Duty Cycle, Peak Transmitter Power, Average transmitter Power.	1.2	3/3	BB		
L4	Illustrative Problems	1.2	3/3	BB		
L5	Simple form of the Radar Equation,	1.3	4/3	BB		
L6	Radar Block Diagram and Operation, Radar Frequencies	1.1	10/3	BB		
L7	Illustrative Problems	1.3	10/3	BB		
L8	Applications of Radar, The Origins of Radar	1.4	10/3	Seminar		
	Module 2					
L9	The Radar Equation: Prediction of Range Performance,	2.1	11/3	BB PPT		
L10	Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR,	2.1	17/3	BB PPT		
L11	Modified Radar Range Equation	2.2	17/3	BB		
L12	Envelope Detector — False Alarm Time and Probability	2.2	24/3	BB PPT		
L13	Probability of Detection	2.2	24/3	BB		
L14	simple targets – sphere, cone-sphere, Transmitter Power	2.3	24/3	BB PPT		
L15	PRF and Range Ambiguities, System Losses	2.4	25/3	BB		
L16	Illustrative Problems	2.2	25/3	BB		
	Module 3					
L17	MTI and Pulse Doppler Radar: Introduction, Principle	3.1	6/4	BB		
L18	Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction	3.1	6/4	BB		

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L19	Delay Line Canceler, MTI Radar with – Power Amplifier Transmitter	3.2	6/4	BB		
L20	Delay Line Cancelers — Frequency Response of Single Delay- Line Canceler	3.2	8/4	BB		
L21	Blind Speeds, Clutter Attenuation, MTI Improvement Factor	3.2	8/4	BB		
L22	N- Pulse Delay-Line Canceler,	3.2	10/4	BB		
L23	Digital MTI Processing – Blind phases, I and Q Channels	3.3	10/4	BB		
L24	Digital MTI Doppler signal processor, Moving Target Detector- Original MTD	3.3	10/4	BB		
	Module 4					
L25	Tracking Radar: Tracking with Radar- Types of Tracking Radar Systems	4.1	13/4	BB PPT		
L26	Monopulse Tracking-Amplitude Comparison Monopulse	4.2	13/4	BB PPT		
L26	Phase Comparison Monopulse.	4.2	17/4	BB		
L28	Sequential Lobing	4.3	17/4	BB		
L29	Conical Scan Tracking	4.3	24/4	BB		
L30	Block Diagram of Conical Scan Tracking Radar	4.3	24/4	BB		
L31	Tracking in Range	4.3	25/4	BB		
L32	Comparison of Trackers.	4.3	25/4	BB		
	Module 5					
L33	The Radar Antenna: Functions of The Radar Antenna	5.1	6/5	Seminar		
L34	Antenna Parameters, Reflector Antennas	5.1	6/5	Seminar		
L35	Electronically Steered Phased array Antennas	5.1	6/5	Seminar		
L36	The Radar Receiver, Receiver Noise Figure	5.2	7/5	Seminar		
L37	Super Heterodyne Receiver	5.2	7/5	Seminar		
L38	Duplexers	5.2	7/5	Seminar		
L39	Radar Displays	5.3	7/5	Seminar		
L40	Receivers Protectors	5.3	7/5	Seminar		

Signature of Faculty Handling/ Course Coordinator/Module Coordinator Date: 17/2

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HOD Date: 26/06/23

2.7 Topics Covered Beyond Syllabus

Date	Topic Covered	Relevant PO	Mode of delivery
10/3	Real time application of Radar	PO1	PPT/Seminar
7/5	Radar Displays with real time images	PO1	PPT/Seminar

2.8 Remedial class Details

S. No.	Date	Topic discussed/numerical problem solved	No. of Students attended
--	---	--	--
--	---	--	--

2.9 Innovative teaching methods adapted

S. No.	Date	Innovative method adapted	Topics covered
1	8/04/2023	Flipped Class Room	Frequency Response of Single DLC and Blind Speed
2	8/04/2023	Flipped Class Room	N-Pulse DLC
3	24/04/2023	Flipped Class Room	Conical Scanning & Sequential Lobing
4	13/04/2023	Flipped Class Room	Monopulse Tracking

3. Assessment of COs

3.1 Assessment Schedule

Date	Assessment Tool Used	TLOs Assessed	Average Cognitive Level
31/03/2023	IA-1	1.1,1.2,1.3, 1.4, 2.1, 2.2, 2.3, 2.4	2.42
20/04/2023	IA-2	3.1, 3.2, 3.3	2.53
11/05/2023	IA-3	4.1, 4.2, 4.3, 5.1, 5.2, 5.3	2.00

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3.2 Measuring CO Attainment

3.2.1 Direct attainment

TLOs mapped	Assessment Tool Used	Attained Level of Bloom's Taxonomy	Marks allotted	Total Marks	Weightage	Attainment Level	Contribution to CO Attainment	CO - Direct attainment
1.1	IA1	L2	7	30	0.23	3	0.7	1.40
1.2	IA1	L2	8		0.27	0	0	
1.3	IA1	L3	8		0.27	0	0	
1.4	IA1	L2	7		0.23	3	0.7	
2.1	IA1	L3	8	30	0.27	1	0.27	2.07
2.2	IA1	L3	12		0.40	3	1.2	
2.3	IA1	L2	6		0.20	1	0.2	
2.4	IA1	L2	4		0.13	3	0.4	
3.1	IA2	L3	38	90	0.42	3	1.27	2.60
3.2	IA2	L3	16		0.18	2	0.36	
3.3	IA2	L2	6		0.07	3	0.2	
4.1	IA3	L2	7		0.08	0	0	
4.2	IA3	L2	8		0.09	3	0.27	
4.3	IA3	L2	15		0.17	3	0.5	
5.1	IA3	L2	7	30	0.23	0	0	2.30
5.2	IA3	L2	8		0.27	3	0.8	
5.3	IA3	L2	15		0.50	3	1.5	

3.2.2 Indirect attainment (Course end survey)

S. No.	CO questions	Number of students responded			Indirect Attainment Level (3*A+2*B+C)/N
		Strongly agree (A)	Agree (B)	Neutral (C)	
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	5	3	0	2.333333333
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2	6	0	2
3	Explain the working and applications of different types of Radar.	1	7	0	1.888888889
4	Describe the working of various radar antennas and receivers.	1	7	0	1.888888889

3.2.3 Final CO attainment

Sl. No.	Course Outcomes	Direct attainment	Indirect attainment	Final CO = 80% DA + 20% IA
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	1.4	2.333333333	**1.59**
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2.07	2	**2.06**

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3	Explain the working and applications of different types of Radar.	2.6	1.888888889	**2.46**
4	Describe the working of various radar antennas and receivers.	2.3	1.888888889	**2.22**

3.3 Observations of Course coordinator on CO attainment

Sl. No.	Course Outcomes	Target	Attainment	Gap	Action Proposed to bridge the Gap	Revision of target wherever achieved
1	Understand the basics of radar system and apply the radar range equation to find the maximum range.	2.2	1.59	0.61	Students should be engaged through online class	2.2
2	Examine the range parameters of Radar system which affect the system performance and also understand Radar Cross Section of Targets	2.2	2.06	0.14	Students should be engaged through online class	2.2
3	Explain the working and applications of different types of Radar.	2.2	2.46	-	-	2.3
4	Describe the working of various radar antennas and receivers.	2.2	2.22		-	2.3

3.4 Other Information

	Section - A
Total number of classes held	40
Number of tutorial classes held	-
Number of seminars held	12
Portion coverage	100
Student's feedback	-
No. of students having attendance shortage	-
University result	100
Use of various teaching methods	Black Board, PPT, Video, Google Classroom
Details of the e-content developed	PPT- 32, YouTube Videos – 09 Google Classroom

3.5 Outcomes on Actions of the Observations/Suggestions of the AY: 2021-22

S. No.	Action Taken	Change Observed
1	Seminar were conducted	More Student involvement
2	Innovative teaching methods used	Students understood the topic well

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3.6 Comments/Suggestions by the Course Coordinator for the next academic year

S. No.	Comment/Observations	Suggested Actions
1	Many Students missed classes due internships opportunities	Students can be engaged through online class.
2	—	---

Remarks by the Module Coordinator CO1 & CO2 target to be retained and revision of CO's are suggested for CO3 & CO4

Signature of Faculty Handling/Course Coordinator/Module Coordinator
Date: 26/6/23

HOD
Date: 26/6/23

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Department: ECE	IA- I	Academic Year: 2021-22
Class: V semester	Course: Verilog HDL	Course Code: 18EC56
Date: 22/11/2021	Duration: 75 minutes	Max. Marks: 30

QP Version: A

Note: Answer the following questions

Qn. No	Question	Marks	PI*	BL*	CO*
1(a)	Explain the typical design flow for designing VLSI IC Circuits.	6	1.3.1	L2	CO1
(b)	Illustrate top-down design methodology with the help of 4-bit ripple counter module.	6	1.4.1	L3	CO1
	OR				
2(a)	Discuss the different levels of abstraction used in Verilog modeling.	6	1.4.1	L2	CO1
(b)	With the help of block diagram, truth table, necessary equations, design block code and stimulus code, implement 2:4 decoder using basic gates.	6	1.3.1	L3	CO1
3(a)	Illustrate the different gates supported by Verilog HDL with the help of truth table consisting of input values '0', '1', 'X' and 'Z'. Also write the Verilog HDL statements to instantiate all the gates.	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A circuit rings a bell whenever motion is detected from one of the two motion sensors. A switch S determines which sensor to pay attention to: S=0 => ring the bell when there's motion at motion sensor 1 S=1 => ring the bell when there's motion at motion sensor 2	6	1.3.1	L4	CO3
(c)	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	6	1.4.1	L3	CO1
	OR				
4(a)	Write gate level description to implement function y= (a. b) +c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	6	1.3.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A car has a fuel-level detector that outputs the current fuel-level as a 3-bit binary number, with 000 meaning empty and 111 meaning full. Using the combinational design process, create a circuit that illuminates a "low fuel" indicator light (by setting an output L to 1) when the fuel level drops below level 3.	6	1.3.1	L4	CO3
(c)	Implement the below problem statement in dataflow modeling. Let variables T represent being tall, H being heavy, and F being fast. Let's consider anyone who is not tall as short, not heavy as light, and not fast as slow. a. You may ride a particular amusement park ride only if you are either tall and light, or short and heavy. b. You may NOT ride an amusement park ride if you are either tall and light, or short and heavy. c. You are eligible to play on a particular basketball team if you are tall and fast, or tall and slow.	6	1.4.1	L3	CO3

BL* Bloom's Taxonomy Level; CO* Course Outcome; PI- Performance Indicator

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QP quality

CO	Maximum Marks	Maximum marks			% questions		
		L2 level questions	L3 level questions	L4 level questions	L2 level questions	L3 level questions	L4 level questions
CO1	30	12	18	0	20	30	0
CO3	30	0	18	12	0	30	20

Overall QP quality = 2 X % of L2 questions + 3 X % of L3 questions + 4 X % of L4 questions
= (2 X 0.2) + (3 X 0.6) + (4 X 0.2)
= 3

Prepared By (Name & signature with date): Ms. Sowmya Bhat
13/11/2021

Remarks by scrutiny team:
Course type (Theoretical/Theoretical & numerical/Numerical)

Scrutinized by (Name & signature with date): HVB Achar
15/11/21

QP selected for the test: YES/NO

HoD Signature with date and seal

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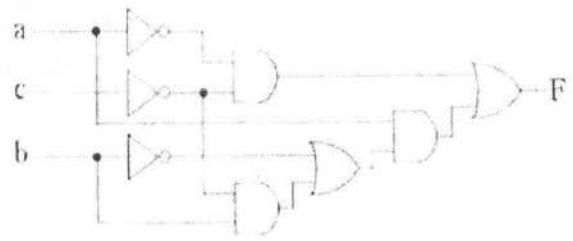
SMVITM

Department: ECE	IA- I	Academic Year: 2021-22
Class: V semester	Course: Verilog HDL	Course Code: 18EC56
Date: 22/11/2021	Duration: 75 minutes	Max. Marks: 30

QP Version: B

Note: Answer the following questions

Qn. No	Question	Marks	PI*	BL*	CO*
1(a)	Explain design flow for designing VLSI IC circuits with a neat flowchart.	6	1.3.1	L2	CO1
(b)	Illustrate bottom-down design methodology with the help of 4-bit ripple counter module.	6	1.4.1	L3	CO1
	OR				
2(a)	Discuss the different components of a simulation used in Verilog modeling.	6	1.4.1	L2	CO1
(b)	With the help of block diagram, truth table, necessary equations, design block code and stimulus code, implement 4:1 Multiplexer using basic gates.	6	1.3.1	L3	CO1
3(a)	Illustrate the different gates supported by Verilog HDL with the help of truth table consisting of input values '0', '1', 'X' and 'Z'. Also write the Verilog HDL statements to instantiate all the gates.	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A museum has three rooms, each with a motion sensor (m0, m1, and m2) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks from room to room. Create a circuit that sounds an alarm (by setting an output A to 1) if motion is ever detected in more than one room at a time (i.e., in two or three rooms), meaning there must be one or more intruders in the museum.	6	1.3.1	L4	CO3
(c)	Let variables S represent a package being small, H being heavy, and E being expensive. Consider a package that is not small as big, not heavy as light, and not expensive as inexpensive. Implement the below problem statement in dataflow modeling. a. You can deliver packages only if the packages are either small and expensive, or big and inexpensive. b. You can NOT deliver a package only if the packages are either small and expensive, or big and inexpensive. c. You can load the packages into your truck only if the packages are small and light, small and heavy, or big and light.	6	1.4.1	L3	CO3
	OR				
4(a)	Implement the below circuit in gate level modeling. 	6	1.4.1	L3	CO3
(b)	Compare and contrast gate level modeling and dataflow modeling using Verilog HDL for the below problem statement: A house has four external doors each with a sensor that outputs 1 if its door is open. Inside the house is a single LED that a homeowner wishes to use to indicate whether a door is open or closed. Because the LED can only show the status of one sensor, the homeowner buys a switch that can be set to 0, 1, 2, or 3 and that has a 2-bit output.	6	1.3.1	L4	CO3

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	representing the switch position in binary. Create a circuit to connect the four sensors, the switch, and the LED.			
(c)	Write gate level description to implement function y=a+(b.c), with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	6	L3	CO2

BL* Bloom's Taxonomy Level; CO* Course Outcome; PI- Performance Indicator

QP quality

CO	Maximum Marks	Maximum marks			% questions		
		L2 level questions	L3 level questions	L4 level questions	L2 level questions	L3 level questions	L4 level questions
CO1	30	12	18	0	20	30	0
CO2	30	0	18	12	0	30	20

Overall QP quality = 2 X % of L2 questions + 3 X % of L3 questions + 4 X % of L4 questions
= (2 X 0.2) + (3 X 0.6) + (4 X 0.2)
= 3

Prepared By (Name & signature with date): Ms. Sowmya Bhat
13/11/2021

Remarks by scrutiny team:
Course type (Theoretical/Theoretical & numerical/Numerical)

Scrutinized by (Name & signature with date): HVB Achar
15/11/21

QP selected for the test: YES/NO

HoD Signature with date and seal

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CBCS SCHEME

USN | | | | | | | | | | BESCK104C/ BESCKC104

First Semester B.E./B.Tech. Degree Examination, Jan./Feb. 2023
Introduction to Electronics and Communication

Time: 3 hrs. Max. Marks: 100

Note: 1. *Answer any FIVE full questions, choosing ONE full question from each module.*
2. *VTU Formula Hand Book is permitted.*
3. *M : Marks , L: Bloom's level , C: Course outcomes.*

		Module – 1	M	L	C
Q.1	a.	Draw the block diagram of DC power supply and explain the individual blocks.	8	L2	CO1
	b.	Draw the circuit diagram of voltage regulation and explain the operation.	6	L2	CO1
	c.	An amplifier produces an output voltage of 2V for an input of 50mV. If the input and output currents in this condition are 1mA and 200mA respectively. Find : i) The voltage gain ii) The current gain iii) The power gain.	6	L3	CO1
		OR			
Q.2	a.	With a neat circuit diagram and waveform Explain the working operation of a full wave bridge rectifier.	8	L2	CO1
	b.	Draw the circuit diagram of voltage doubler and the working operation.	6	L2	CO1
	c.	Discuss briefly a Negative feedback amplifier with block diagram.	6	L1	CO1
		Module – 2			
Q.3	a.	With circuit diagram, explain the operation of an wien bridge oscillator.	8	L2	CO2
	b.	Define the following operational amplifier parameters value. i) Open loop voltage gain ii) Output Resistance iii) Slew Rate	6	L1	CO2
	c.	Draw the circuit diagram and input and output waveform of the following operational amplifier circuits i) Differentiators ii) Integrator.	6	L1	CO2
		OR			
Q.4	a.	Explain the single state astable oscillator with circuit diagram.	8	L1	CO2
	b.	What is oscillator? And mention condition for oscillations.	6	L1	CO2
	c.	Explain the operation of summing amplifier using operational amplifier and write the output equation.	6	L2	CO2

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		Module – 3			
Q.5	a.	Implement full adder using two half adders and one OR gate. Write the equations for Sum and C_{out}.	8	L3	CO3
	b.	Convert the following numbers to its equivalent numbers and show the steps. i) $(10110001101011.111100000)_2 = (?)_8$ ii) $(10110001101011.11110010)_2 = (?)_{16}$ iii) $(1010.011)_2 = (?)_{10}$	6	L2	CO3
	c.	Using basic Boolean theorems prove i) $(x + y)(x + z) = x + yz$ ii) $xy + xz + y\bar{z} = xz + y\bar{z}$	6	L3	CO3
		OR			
Q.6	a.	Express the Boolean function i) $F = A + \bar{B}C$ in a sum of minterms form ii) $F = xy + \bar{x}z$ in a product of maxterms form.	8	L2	CO3
	b.	Subtract the following using 10's complement i) $(72532 - 3250)_{10}$ ii) $(3250 - 72532)_{10}$	6	L2	CO3
	c.	Write the step by step procedure to design a combinational circuit.	6	L1	CO3
		Module – 4			
Q.7	a.	What is an Embedded system? Compare Embedded systems with general computer systems.	8	L2	CO4
	b.	Mention the classification of Embedded system based on complexity and performance.	6	L1	CO4
	c.	Write a short note on – 7-segment LED display.	6	L2	CO4
		OR			
Q.8	a.	Discuss the typical embedded system elements.	8	L2	CO4
	b.	What is the difference between RISC and CISC processors?	6	L1	CO4
	c.	Write a short note on : i) Transducers ii) Sensors.	6	L2	CO4
		Module – 5			
Q.9	a.	Draw the block diagram of basic communication system and briefly explain the individual blocks.	10	L2	CO5
	b.	Discuss the types of communication systems.	5	L2	CO5
	c.	List the advantages of digital communication over analog communication.	5	L1	CO5
		OR			
Q.10	a.	Define Amplitude and Frequency modulation. Sketch AM and FM waveform.	10	L1	CO5
	b.	Write a short note on : Amplitude Shift Keying (ASK) modulator and demodulator.	10	L2	CO5

* * * * *

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Vishwothama Nagar, Bantakal – 574115, Udupi District, Karnataka

SMVITM

IPCC BEC302 - Digital System Design using Verilog LAB

LABORATORY MANUAL

IVTH SEMESTER B.E. (ECE)

NAME OF THE STUDENT : _____

UNIVERSITY SEAT NUMBER : _____

SECTION & BATCH : _____

Prepared by: Ms Sowmya Bhat

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Department Vision:

To be recognized as a center of eminence in the field of Electronics and Communication Engineering for holistic engineering education and research on current technologies.

Department Mission:

1. Impart quality engineering education with ethics to students and transform them into leaders in technology, innovation and research.
2. Provide a platform and academic atmosphere that will ensure the transfer of knowledge and skills to the students.
3. Promote the overall personality development of the students through activities that have high credibility and societal impact.

Programme Educational Objectives:

The graduate of Electronics and Communication Engineering should be able to

PEO-1 Exhibit essential knowledge of applied sciences, mathematical modelling, logical interpretation and virtual realization to resolve real-time problems in the field of Electronics and Communication Engineering

PEO-2 Work productively as an Electronics and Communication Engineer, including supportive and leadership roles on multidisciplinary teams.

PEO-3 Inculcate effective communication skills to excel in professional growth.

PEO-4 Take part in lifelong learning in pace with the advancing technological society.

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DIGITAL SYSTEM DESIGN USING VERILOG LAB

B.E., III Semester, Electronics & Communication Engineering

2022 Scheme

Course Code	BEC302	**CIE Marks**	25
Exam duration	2/3 hours		

Course Objectives

This course will enable the students to:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

S.No.	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description: 8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder, 2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type
8	To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

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Course Outcomes

At the end of the course the student will be able to:

1. Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
2. Analyze and design for combinational logic circuits.
3. Analyze the concepts of Flip Flops (SR, D,T and JK) and to design the synchronous sequential circuits using Flip Flops.
4. Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks**).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.

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- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test (**duration 02/03 hours**) after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks**.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

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3	To realize 4-bit ALU using Verilog program.	12
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa	14
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder	20
6	To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder,2 – bit Comparator	24
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d)D type	28
8	To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.	32
	Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).	34
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.	35
	Content Beyond Syllabus	36

Reference Books:

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3. Fundamentals of HDL,by Cyril PR, Pearson/Sanguine2010

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Experiment No: 1

AIM: To simplify the given Boolean expressions and realize using Verilog program

Y1= A′ B′ + AB + A′ B

Y2= (A + B) (A + B′)

Y3= A′ B + AB′ + A′ B′ +AB

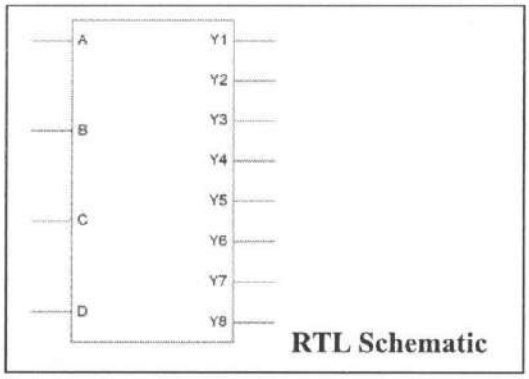
Y4= AB′ + B′ C′ + A′ C′

Y5= A′ BC + AC

Y6= AB + A (CD + CD′)

Y7= (BC′ + A′ D) (AB′ + CD′)

Y8=A′ BC + AB′ C′ + A′ B′ C′ +ABC



RTL Schematic

Top Module Program for Boolean Expression

```
module bool (A, B, C, D, Y1, Y2, Y3, Y4, Y5,
Y6, Y7, Y8);
input A,B,C,D;
output Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
assign Y1= ~A | B;
assign Y2= A;
assign Y3= 1;
assign Y4= (A& (~B)) | ((~A) & (~C));
assign Y5= C & (A | B);
assign Y6= A & (B | C);
assign Y7= 0;
assign Y8= (B & C) | ((~B) & (~C));
endmodule
```

Testbench Code for Boolean Expression

```
module bool_test;
reg A, B, C, D;
wire Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8;
bool uut (.A(A),.B(B),.C(C),.D(D),
.Y1(Y1), .Y2(Y2), .Y3(Y3), .Y4(Y4),
.Y5(Y5), .Y6(Y6), .Y7(Y7), .Y8(Y8) );
initial
begin
A=0; B=0; C=0; D=0;
end
always
begin
#10 D=!D;
#20 C=!C;
#40 B=!B;
#80 A=!A;
end
initial
begin
#100 $finish;
end
endmodule
```

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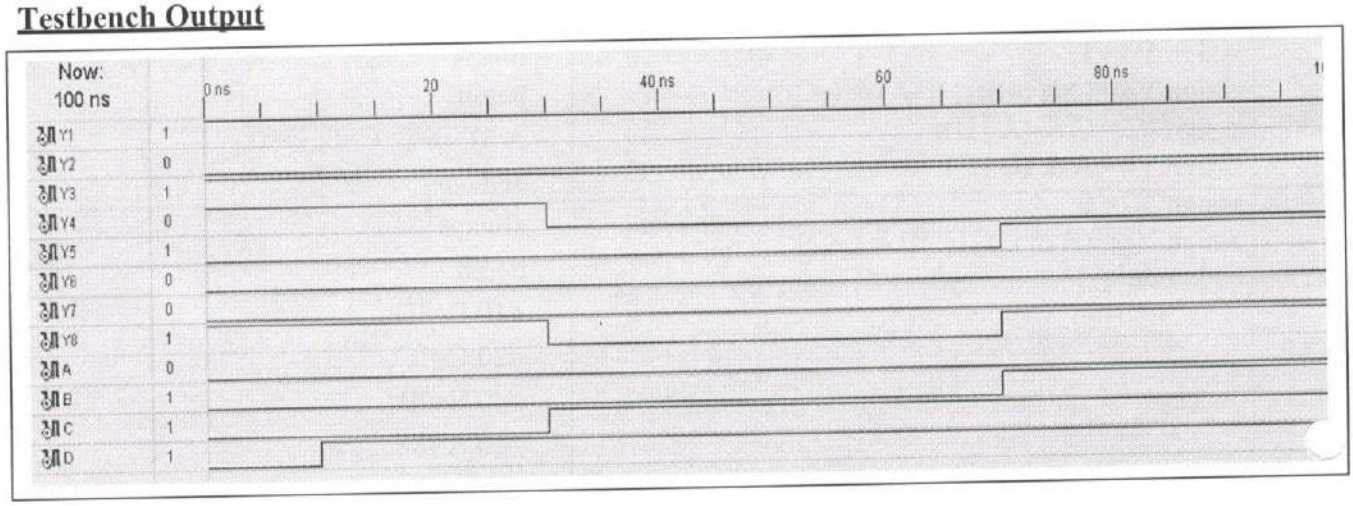
Truth Table

Inputs				Outputs							
A	B	C	D	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	1	0	1	1	0	0	0	1
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	1	0	1	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	0
0	1	0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	1	0	1	0	1	0	0	1
0	1	1	1	1	0	1	0	1	0	0	1
1	0	0	0	0	1	1	1	0	0	0	1
1	0	0	1	0	1	1	1	0	0	0	1
1	0	1	0	0	1	1	1	1	1	0	0
1	0	1	1	0	1	1	1	1	1	0	0
1	1	0	0	1	1	1	0	0	1	0	0
1	1	0	1	1	1	1	0	0	1	0	0
1	1	1	0	1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	0	1	1	0	1

Testbench Output



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Experiment No: 2

AIM: To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.

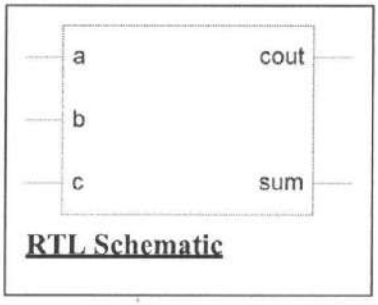
Top Module Code for Full Adder

```
module fulladder (sum,cout, a, b, c);
output sum, cout;
input a, b,c;
assign sum= a ^ b ^ c;
assign cout= (a & b) | (b & c) | (c & a);
endmodule
```

Testbench Code for Full Adder

```
module fulladder_test;
reg a,b,c;
wire sum,cout;
fulladder uut
(.a(a),.b(b),.c(c),.sum(sum),.cout(cout));
initial
begin
a=0;b=0;c=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
always
#5 c=!c;
initial

begin
#100 $finish;
end
endmodule
```



RTL Schematic

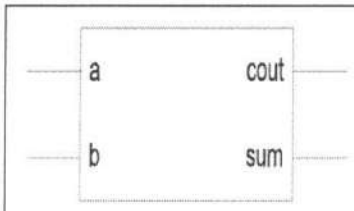
Top Module Code for Half Adder

```
module halfadder (sum,cout, a, b);
output sum, cout;
input a, b;
assign sum= a ^ b;
assign cout= (a & b);
endmodule
```

Testbench Code for Half Adder

```
module halfadder_test;
reg a,b;
wire sum,cout;
halfadder uut
(.a(a),.b(b),.sum(sum),.cout(cout));
initial
begin
a=0;b=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
initial

begin
#100 $finish;
end
endmodule
```



RTL Schematic

Top Module Code for Full Subtractor

```
module fullsubtractor (diff,bout, a, b, bin);
output diff, bout;
input a, b,bin;
assign diff= a ^ b ^ bin;
assign bout= (~a & bin) | (~a & b) | (b &
bin);
endmodule
```

Top Module Code for Half Subtractor

```
module halfsubtractor (diff,bout, a,
b);
output diff,bout;
input a, b;
assign diff= a ^ b;
assign bout= (~a & b);
```

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	endmodule

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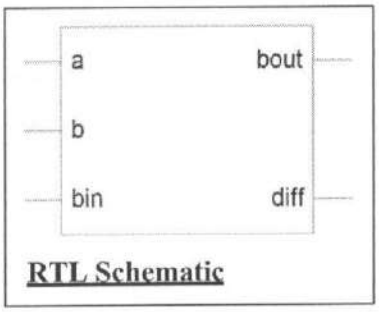
Vishwo

Testbench Code for Full Subtractor

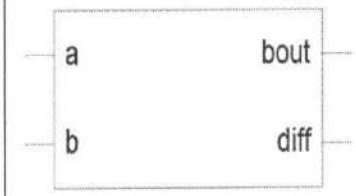
```
module fullsubtractor_test;
reg a,b,bin;
wire diff, bout;
fullsubtractor uut
(.a(a),.b(b),.bin(bin),.diff(diff),.bout(bout));
initial
begin
a=0;b=0;bin=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
always
#5 bin=!bin;
initial
begin
#100 $finish;
end
endmodule
```



RTL Schematic

Testbench Code for Half Subtractor

```
module halfsubtractor_test;
reg a,b;
wire diff, bout;
halfsubtractor uut
(.a(a),.b(b),.diff(diff),.bout(bout));
initial
begin
a=0;b=0;
#10 b=!b;
#10 b=!b;a=!a;
#10 b=!b;
#10 a=!a;
end
initial
begin
#100 $finish;
end
endmodule
```



RTL Schematic

Truth Table

Inputs		Half Adder Outputs		Half Subtractor Outputs	
a	b	cout	sum	bout	diff
0	0	0	0	0	0
0	1	0	1	1	1
1	0	0	1	0	1
1	1	1	0	0	0

Inputs			Full Adder Outputs		Full Subtractor Outputs	
a	b	c/bin	cout	sum	bout	diff
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	1	1	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

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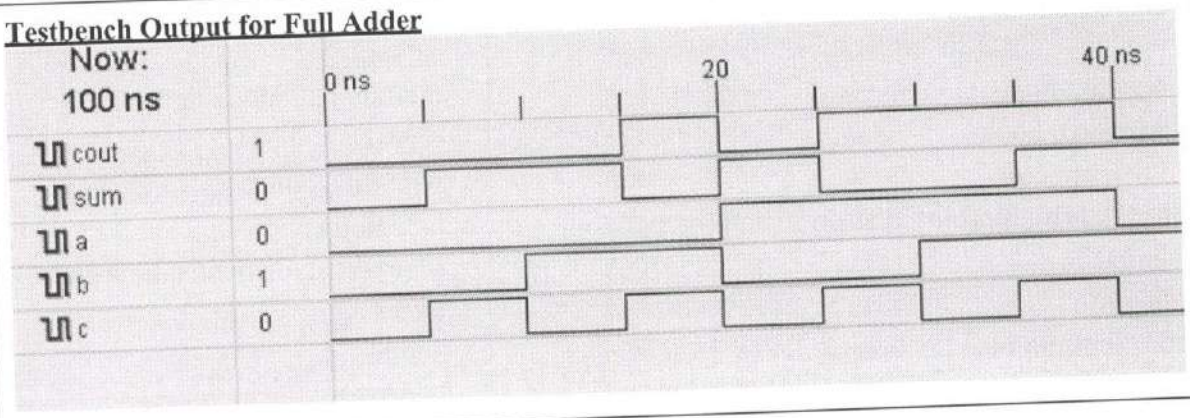
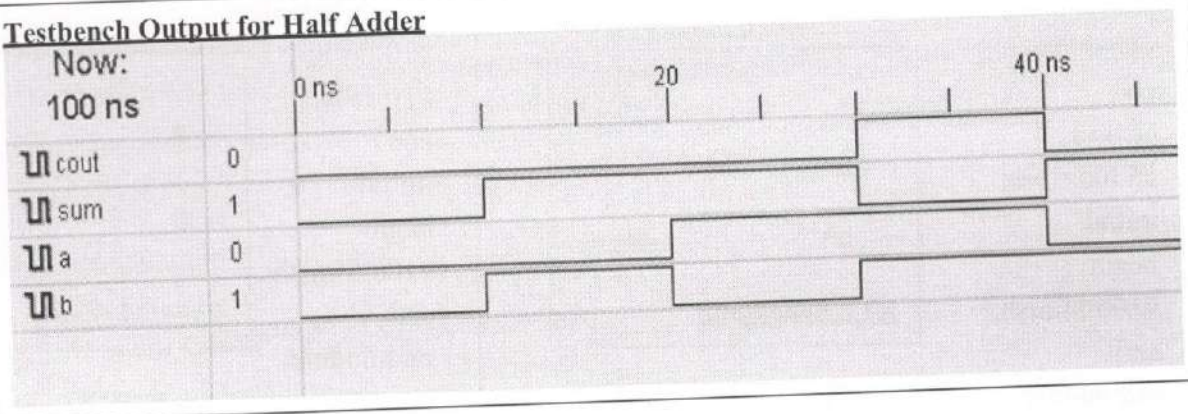
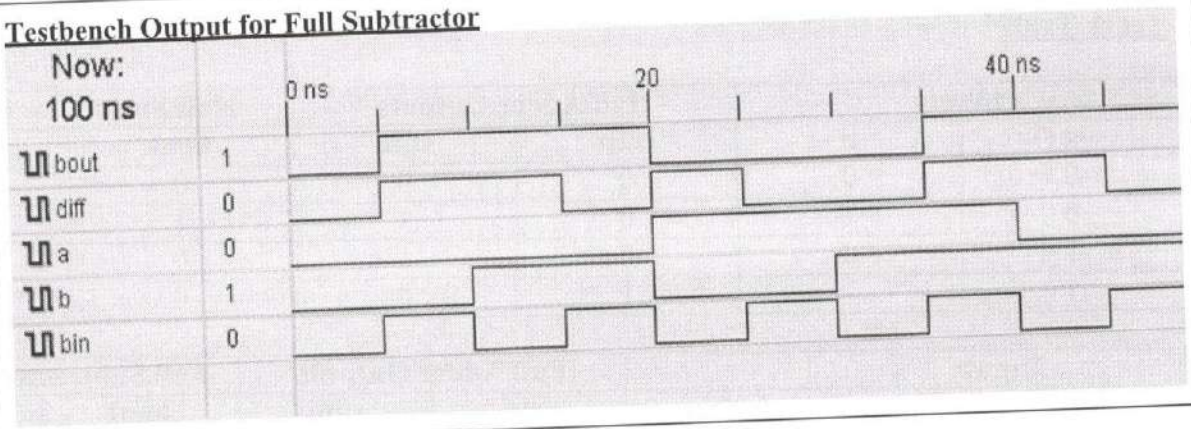
Testbench Output for Full Adder



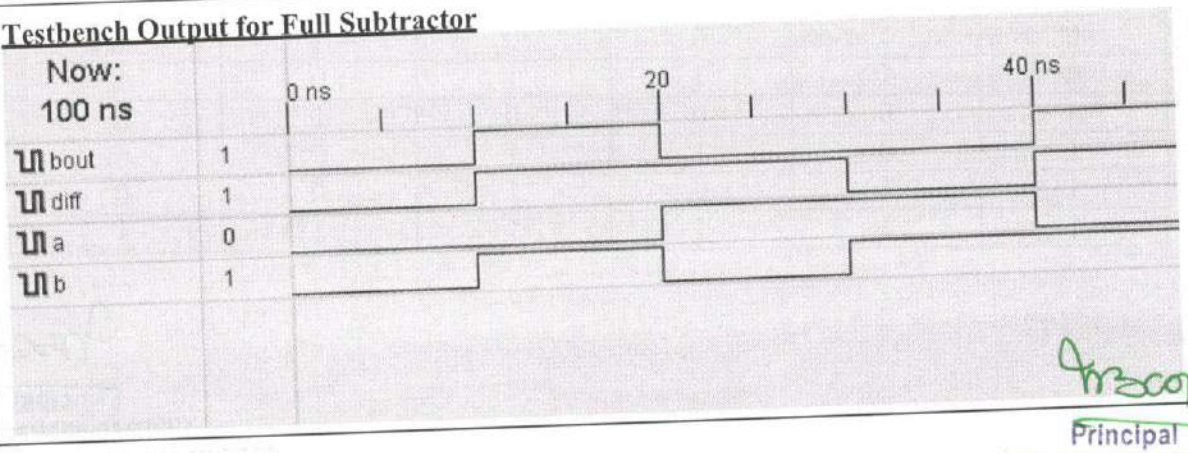
Testbench Output for Half Adder



Testbench Output for Full Subtractor



Testbench Output for Full Subtractor



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Experiment No: 3

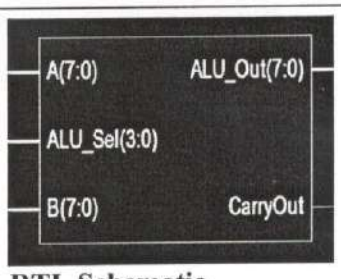
AIM: To realize 4-bit ALU using Verilog program.

Top Module Code for 4-bit ALU

```
module alu(A,B, ALU_Sel, ALU_Out,
CarryOut);
input [7:0] A, B;
input [3:0] ALU_Sel;
output [7:0] ALU_Out;
output CarryOut;
reg [7:0] ALU_Result;
wire [8:0] tmp;
assign ALU_Out = ALU_Result;
assign tmp = {1'b0,A} + {1'b0,B};
assign CarryOut = tmp[8];
always @ (ALU_Sel)
begin
case (ALU_Sel)
4'b0000: ALU_Result = A + B;
4'b0001: ALU_Result = A - B;
4'b0010: ALU_Result = A * B;
4'b0011: ALU_Result = ~A;
4'b0100: ALU_Result = A<<1;
4'b0101: ALU_Result = A>>1;
4'b0110: ALU_Result = {A [6:0], A [7]};
4'b0111: ALU_Result = {A [0], A [7:1]};
4'b1000: ALU_Result = A & B;
4'b1001: ALU_Result = A | B;
4'b1010: ALU_Result = A ^ B;
4'b1011: ALU_Result = ~ (A | B);
4'b1100: ALU_Result = ~ (A & B);
4'b1101: ALU_Result = ~ (A ^ B);
4'b1110: ALU_Result = (A>B)?8'd1:8'd0;
4'b1111: ALU_Result = (A==B)?8'd1:8'd0;
default: ALU_Result = A + B;
endcase
end
endmodule
```

Testbench Code for 4-bit ALU

```
module alu_test;
reg [7:0] A, B;
reg [3:0] ALU_Sel;
wire [7:0] ALU_Out;
wire CarryOut;
alu uut(.A(A),
.B(B),.ALU_Sel(ALU_Sel),.ALU_Out(ALU_Out),
.CarryOut(CarryOut));
initial
begin
A=8'b10101011; B=8'b01010101;
ALU_Sel =4'b0000; #5;
ALU_Sel =4'b0001; #5;
ALU_Sel =4'b0010; #5;
ALU_Sel =4'b0011; #5;
ALU_Sel =4'b0100; #5;
ALU_Sel =4'b0101; #5;
ALU_Sel =4'b0110; #5;
ALU_Sel =4'b0111; #5;
ALU_Sel =4'b1000; #5;
ALU_Sel =4'b1001; #5;
ALU_Sel =4'b1010; #5;
ALU_Sel =4'b1011; #5;
ALU_Sel =4'b1100; #5;
ALU_Sel =4'b1101; #5;
ALU_Sel =4'b1110; #5;
ALU_Sel =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```



RTL Schematic

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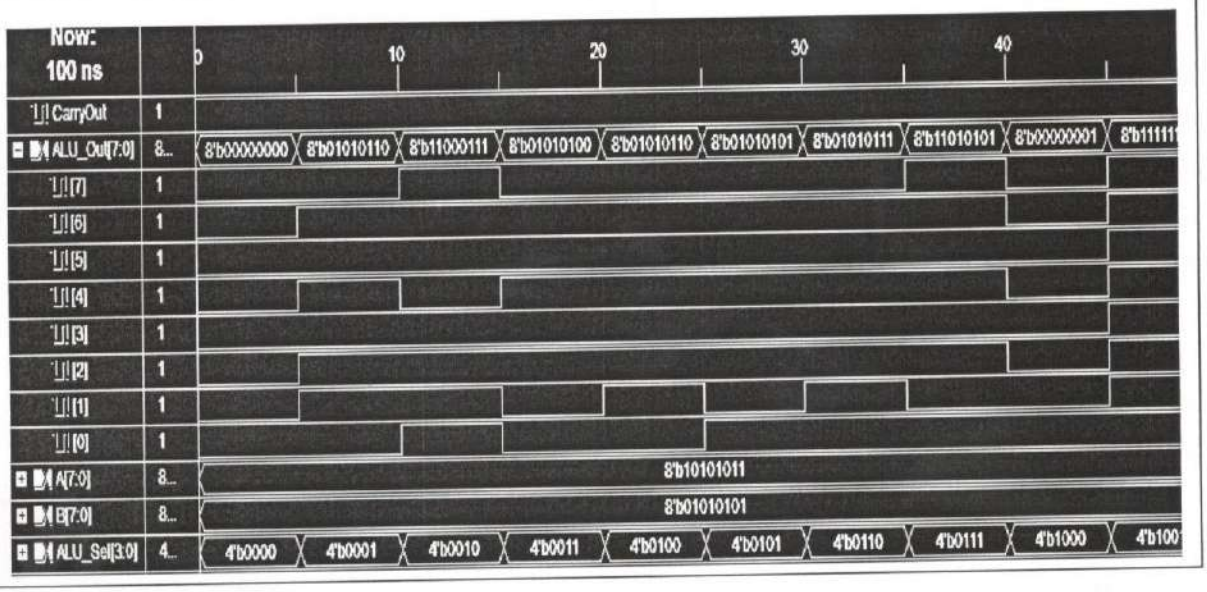
Opcode

ALU_Sel	ALU_Result
0000	A + B - Addition
0001	A – B - Subtraction
0010	A * B - Mutiplication
0011	~A - Complement
0100	A<<1 – logical shift left
0101	A>>1 – logical shift right
0110	{A [6:0], A [7]} – Rotate left
0111	{A [0], A [7:1]} – Rotate right
1000	A & B – logical AND
1001	A | B – logical OR
1010	A ^ B – logical EXOR
1011	~ (A | B) – logical NOR
1100	~ (A & B) – logical NAND
1101	~ (A ^ B) – logical EXNOR
1110	(A>B)?8'd1:8'd0 – greater comparison
1111	(A==B)?8'd1:8'd0 – equal comparison
default	A + B

Testbench Output for 4-bit ALU



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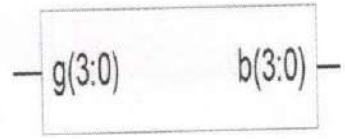
Experiment No: 4

AIM: To realize the following Code converters using Verilog Behavioral description

a) Gray to binary and vice versa b) Binary to excess3 and vice versa

Top Module Code for Gray to Binary

```
module gray_to_binary (g,b);
input [3:0] g;
output [3:0] b;
reg [3:0] b;
always@(g)
begin
b[3] =g[3];
b[2] =b[3] ^ g[2];
b[1] =b[2] ^ g[1];
b[0] =b[1] ^ g[0];
end
endmodule
```



RTL Schematic

Testbench Code for Gray to Binary

```
module gray_to_binary_test;
reg [3:0] g;
wire [3:0] b;
gray_to_binary uut(.g(g), .b(b));
initial
begin
g =4'b0000; #5;
g =4'b0001; #5;
g =4'b0010; #5;
g =4'b0011; #5;
g =4'b0100; #5;
g =4'b0101; #5;
g =4'b0110; #5;
g =4'b0111; #5;
g =4'b1000; #5;
g =4'b1001; #5;
g =4'b1010; #5;
g =4'b1011; #5;
g =4'b1100; #5;
g =4'b1101; #5;
g =4'b1110; #5;
g =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

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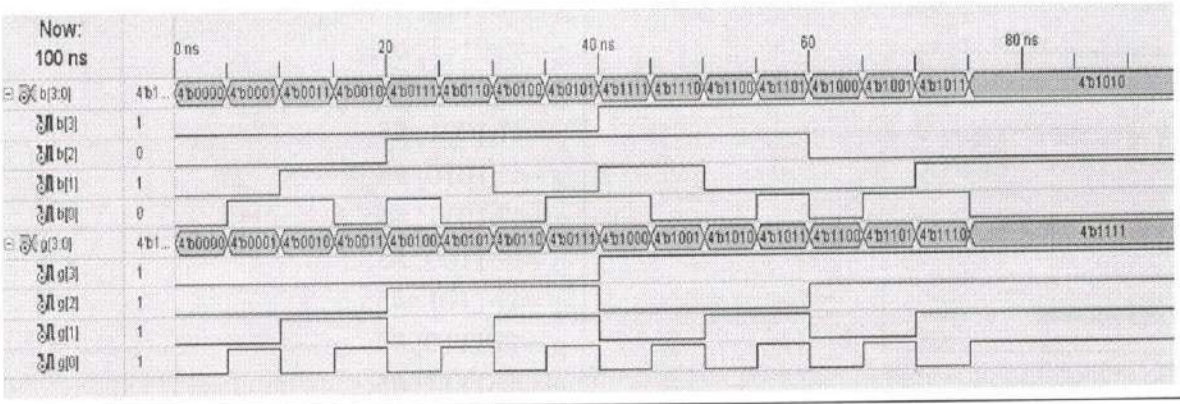
Truth Table

Inputs				Outputs			
g3	g2	g1	g0	b3	b2	b1	b0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Testbench Output for Gray to Binary



Top Module Code for Binary to Gray

```
module binary_to_gray (b, g);
input [3:0] b;
output [3:0] g;
reg [3:0] g;
always@(b)
begin
g[3] = b[3];
g[2] = b[3] ^ b[2];
g[1] = b[2] ^ b[1];
g[0] = b[1] ^ b[0];
end
endmodule
```

Testbench Code for Binary to Gray

```
module binary_to_gray _test;
reg [3:0] b;
wire [3:0] g;
binary_to_gray  uut(.b(b), .g(g));
initial
begin
b =4'b0000; #5;
b =4'b0001; #5;
b =4'b0010; #5;
b =4'b0011; #5;
b =4'b0100; #5;
b =4'b0101; #5;
b =4'b0110; #5;
b =4'b0111; #5;
```

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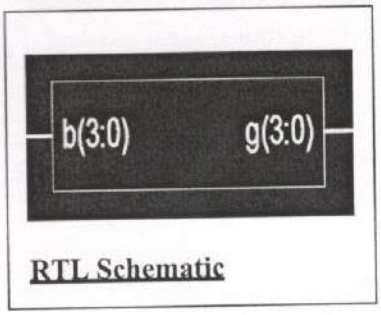


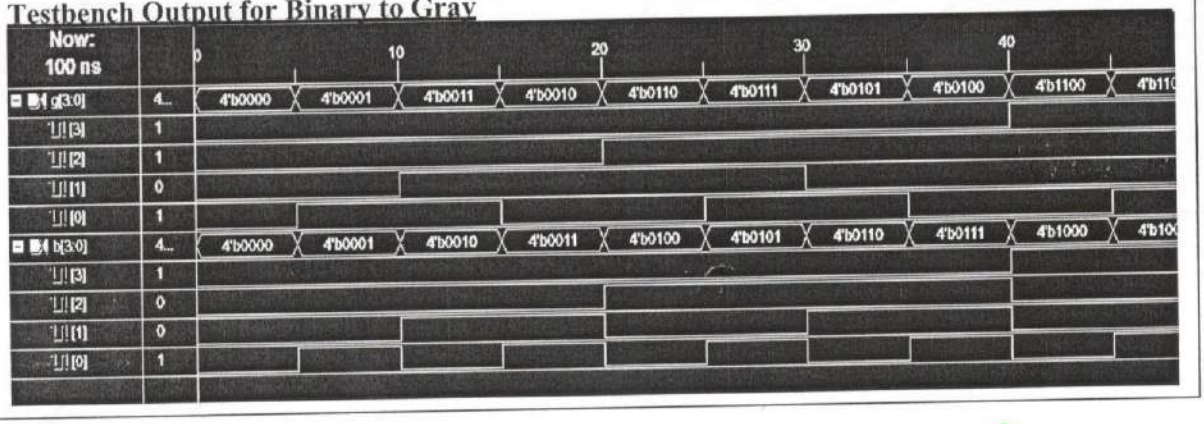
RTL Schematic

```
b =4'b1000; #5;
b =4'b1001; #5;
b =4'b1010; #5;
b =4'b1011; #5;
b =4'b1100; #5;
b =4'b1101; #5;
b =4'b1110; #5;
b =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs			
b3	b2	b1	b0	g3	g2	g1	g0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Testbench Output for Binary to Gray



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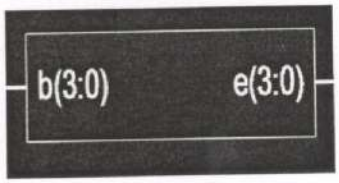
Top Module Code for Binary to Excess3

```
module binary_to_excess3 (b,e);
input [3:0] b;
output [3:0] e;
assign e = (b==0) ? 3: (b==1) ? 4: (b==2)
? 5: (b==3) ? 6: (b==4) ? 7: (b==5) ? 8:
(b==6) ? 9: (b==7) ? 10: (b==8) ? 11:
(b==9) ? 12: (b==10) ? 13 : (b==11) ? 14:
(b==12) ? 15: 4'bzzzz;
endmodule
```



RTL Schematic

Testbench Code for Binary to Excess3

```
module binary_to_excess3_test;
reg [3:0] b;
wire [3:0] e;
binary_to_excess3 uut(.b(b), .e(e));
initial
begin
b =4'b0000; #5;
b =4'b0001; #5;
b =4'b0010; #5;
b =4'b0011; #5;
b =4'b0100; #5;
b =4'b0101; #5;
b =4'b0110; #5;
b =4'b0111; #5;
b =4'b1000; #5;
b =4'b1001; #5;
b =4'b1010; #5;
b =4'b1011; #5;
b =4'b1100; #5;
b =4'b1101; #5;
b =4'b1110; #5;
b =4'b1111; #5;end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs			
b3	b2	b1	b0	e3	e2	e1	e0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	1	1	1
1	1	0	1	z	z	z	z
1	1	1	0	z	z	z	z
1	1	1	1	z	z	z	z

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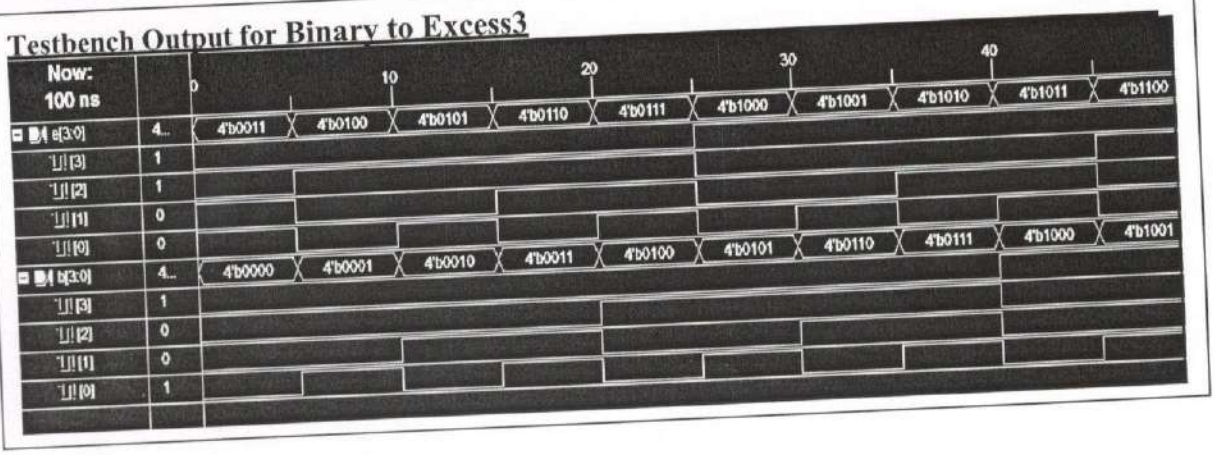
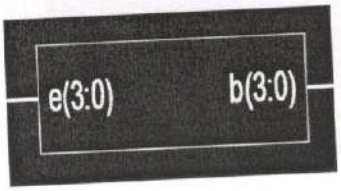
Testbench Output for Binary to Excess3



Top Module Code for Excess3 to Binary

```
module excess3_to_binary (e, b);
input [3:0] e;
output [3:0] b;
assign b  = (e==3) ? 0: (e==4) ? 1: (e==5)
? 2: (e==6) ? 3: (e==7) ? 4: (e==8) ? 5:
(e==9) ? 6: (e==10) ? 7 : (e==11) ? 8:
(e==12) ? 9: 4'bzzzz;
endmodule
```



RTL Schematic

Testbench Code for Excess3 to Binary

```
module excess3_to_binary_test;
reg [3:0] e;
wire [3:0] b;
excess3_to_binary uut(.b(b), .e(e));
initial
begin
e =4'b0000; #5;
e =4'b0001; #5;
e =4'b0010; #5;
e =4'b0011; #5;
e =4'b0100; #5;
e =4'b0101; #5;
e =4'b0110; #5;
e =4'b0111; #5;
e =4'b1000; #5;
e =4'b1001; #5;
e =4'b1010; #5;
e =4'b1011; #5;
e =4'b1100; #5;
e =4'b1101; #5;
e =4'b1110; #5;
e =4'b1111; #5;
end
initial
begin
#100 $finish;
end
endmodule
```

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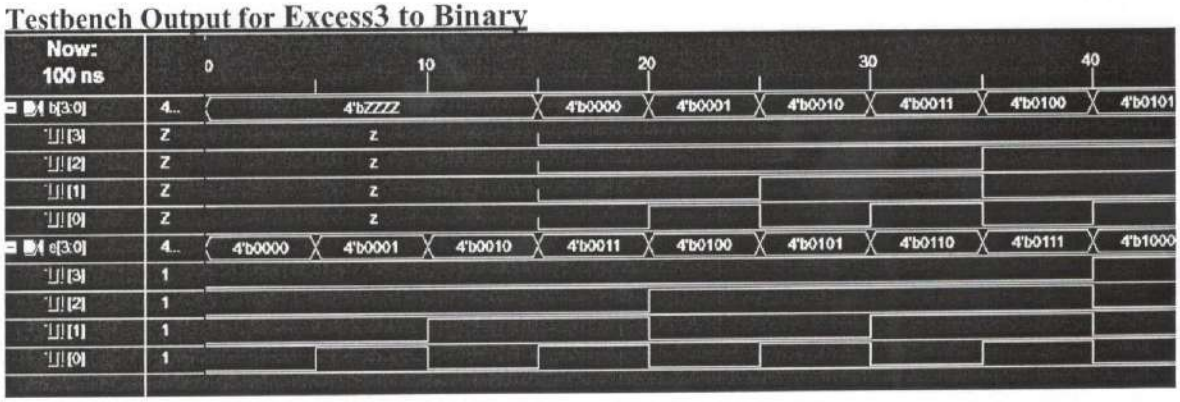
Truth Table

Inputs				Outputs			
e3	e2	e1	e0	b3	b2	b1	b0
0	0	0	0	z	z	z	z
0	0	0	1	z	z	z	z
0	0	1	0	z	z	z	z
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

Testbench Output for Excess3 to Binary



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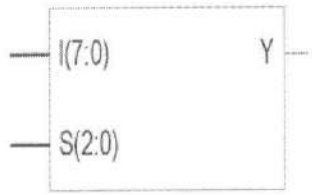
Experiment No: 5

AIM: To realize using Verilog Behavioral description: 8:1mux, 8:3encoder, Priority encoder

Top Module Code for 8:1 MUX

```
module 8_1_mux(Y, I, S);
output Y;
input [7:0] I;
input [2:0] S;
always@ (S, I)
begin
if (S==3'b000)
Y=I[0];
else if (S==3'b001)
Y=I[1];
else if (S==3'b010)
Y=I[2];
else if (S==3'b011)
Y=I[3];
else if (S==3'b100)
Y=I[4];
else if (S==3'b101)
Y=I[5];
else if (S==3'b110)
Y=I[6];
else if (S==3'b111)
Y=I[7];
else Y=1'bZ;
end
endmodule
```

RTL Schematic



Testbench Code for 8:1 MUX

```
module 8_1_mux_test;
reg [7:0] I;
reg [2:0] S;
wire Y;
8_1_mux uut(.I(I), .S(S), .Y(Y));
initial
begin
S=3'b000; I=8'b10010001; #10;
S=3'b001; #10;
S=3'b010; #10;
S=3'b011; #10;
S=3'b100; #10;
S=3'b101; #10;
S=3'b110; #10;
S=3'b111; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Output
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

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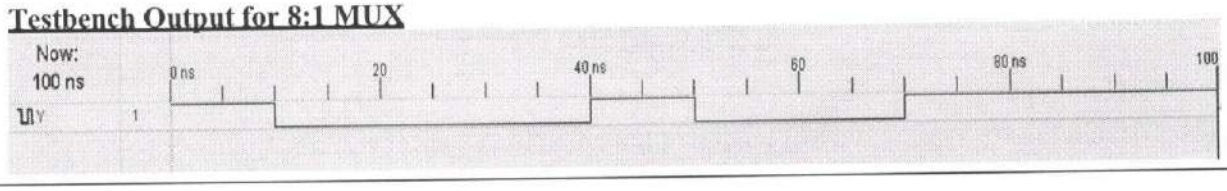
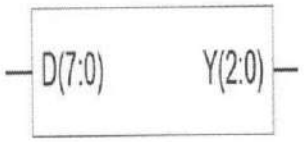
Testbench Output for 8:1 MUX



Top Module Code for 8:3 Encoder

```
module 8_3_encoder(Y, D);
input [7:0]D;
output [2:0]Y;
reg [2:0] Y;
always@ (D)
begin
case(D)
8'b00000001: Y=3'b000;
8'b00000010: Y=3'b001;
8'b00000100: Y=3'b010;
8'b00001000: Y=3'b011;
8'b00010000: Y=3'b100;
8'b00100000: Y=3'b101;
8'b01000000: Y=3'b110;
8'b10000000: Y=3'b111;
endcase
end
endmodule
```

RTL Schematic



Testbench Code for 8:3 Encoder

```
module 8_3_encoder_test;
reg [7:0] D;
wire [2:0] Y;
8_3_encoder uut(.D(D),.Y(Y));
initial
begin
D=8'b00000000; #10;
D=8'b00000010; #10;
D=8'b00000100; #10;
D=8'b00001000; #10;
D=8'b00010000; #10;
D=8'b00100000; #10;
D=8'b01000000; #10;
D=8'b10000000; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs								Outputs		
D7	D6	D5	D4	D3	D2	D1	D0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

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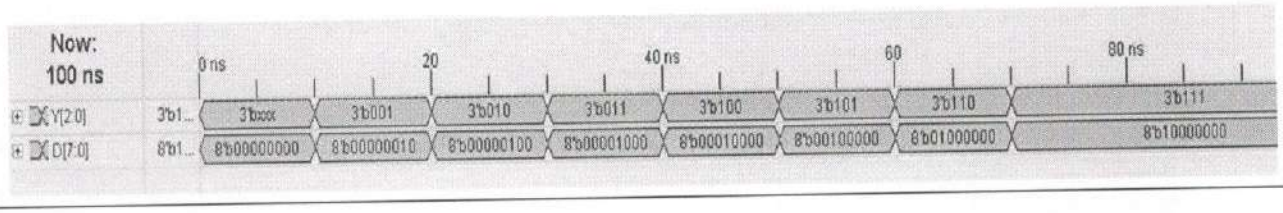
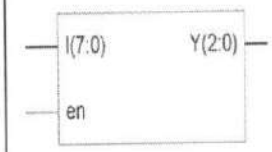
Testbench Output for 8:3 Encoder



Top Module Code for Priority Encoder

```
module 8_3_priorityencoder(Y, I, en);
output [2:0] Y;
input [7:0] I;
input en;
reg [2:0] Y;
always@ (en, I)
begin
if (en==1)
begin
if (I[7]==1) Y=3'b111;
else if (I[6]==1) Y=3'b110;
else if (I[5]==1) Y=3'b101;
else if (I[4]==1) Y=3'b100;
else if (I[3]==1) Y=3'b011;
else if (I[2]==1) Y=3'b010;
else if (I[1]==1) Y=3'b001;
else
Y=3'b000;
end
else Y=3'bzzz;
end
endmodule
```

RTL Schematic



Testbench Code for Priority Encoder

```
module 8_3_priorityencoder_test;
reg [7:0] I;
reg en;
wire [2:0] Y;
8_3_priorityencoder uut (.en(en), .I(I),
.Y(Y));
initial
begin
en=1;I=8'b1XXXXXXX; #10;
I=8'b01XXXXXX; #10;
I=8'b001XXXXX; #10;
I=8'b0001XXXX; #10;
I=8'b00001XXX; #10;
I=8'b000001XX; #10;
I=8'b0000001X; #10;
I=8'b00000001; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs								Outputs		
I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

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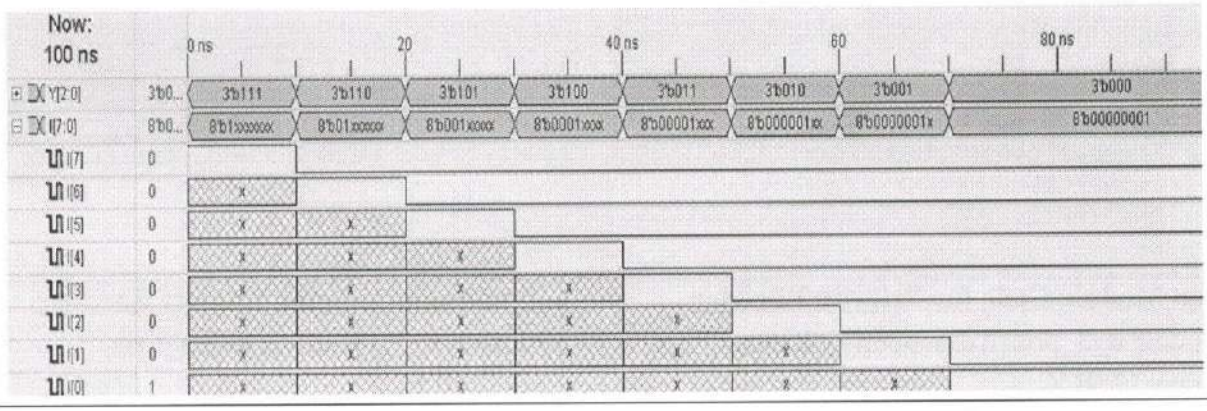
Testbench Output for Priority Encoder



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Experiment No: 6

AIM: To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder, 2 –bit Comparator

Top Module Code for 1:8 Demux

```
module 1_8_demux (i, s2, s1, s0, y);
output [7:0] y;
input i, s2, s1, s0;
reg [7:0] y;
always@ (i or s2 or s1 or s0)
begin
case ({s2, s1, s0})
0: y[0]=i;
1: y[1]=i;
2: y[2]=i;
3: y[3]=i;
4: y[4]=i;
5: y[5]=i;
6: y[6]=i;
7: y[7]=i;
endcase
end
endmodule
```

Testbench Code for 1:8 Demux

```
module 1_8_demux_test;
reg i, s2, s1, s0;
wire [7:0] y;
1_8_demux uut(.i(i),.s2(s2), .s1(s1), .s0(s0),
.y(y));
initial
begin
i=0; #10;
i=1; s2=0; s1=0; s0=0; #10;
s2=0; s1=0; s0=1; #10;
s2=0; s1=1; s0=0; #10;
s2=0; s1=1; s0=1; #10;
s2=1; s1=0; s0=0; #10;
s2=1; s1=0; s0=1; #10;
s2=1; s1=0; s0=0; #10;
s2=1; s1=1; s0=1; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Outputs							
S2	**S1**	**S0**	**Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**
0	0	0	0	0	0	0	0	0	0	i
0	0	1	0	0	0	0	0	0	i	0
0	1	0	0	0	0	0	0	i	0	0
0	1	1	0	0	0	0	i	0	0	0
1	0	0	0	0	0	i	0	0	0	0
1	0	1	0	0	i	0	0	0	0	0
1	1	0	0	i	0	0	0	0	0	0
1	1	1	i	0	0	0	0	0	0	0

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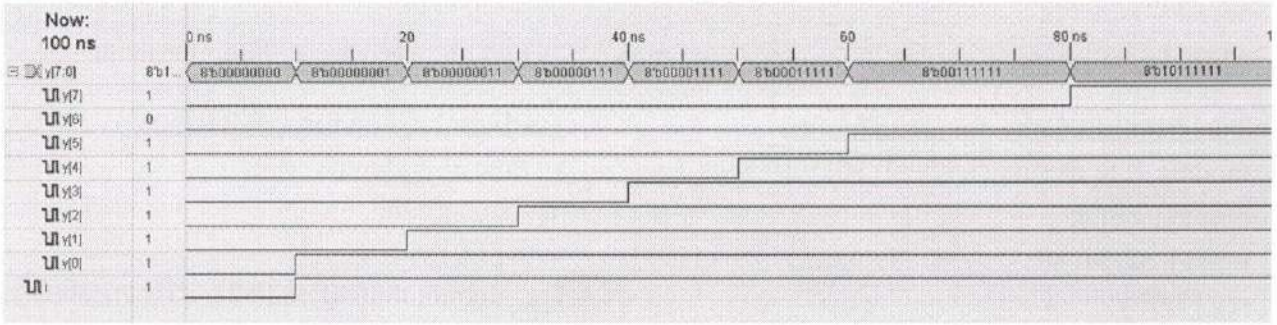
Testbench Output for 1:8 Demux



Top Module Code for 3:8 Decoder

```
module 3_8_decoder(Y, D);
output [7:0] Y;
input [2:0] D;
reg [7:0] Y;
always@ (D)
begin
case(D)
case(D)
3'b000: Y =8'b00000001;
3'b001: Y =8'b00000010;
3'b010: Y =8'b00000100;
3'b011: Y =8'b00001000;
3'b100: Y =8'b00010000;
3'b101: Y =8'b00100000;
3'b110: Y =8'b01000000;
3'b111: Y =8'b10000000;
endcase
end
endmodule
```

Testbench Code for 3:8 Decoder

```
module 3_8_decoder_test;
reg [2:0] D;
wire [7:0] Y;
3_8_decoder uut(.D(D),.Y(Y));
initial
begin
D=3'b000; #10;
D=3'b001; #10;
D=3'b010; #10;
D=3'b011; #10;
D=3'b100; #10;
D=3'b101; #10;
D=3'b110; #10;
D=3'b111; #10;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs			Outputs							
D2	D1	D0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

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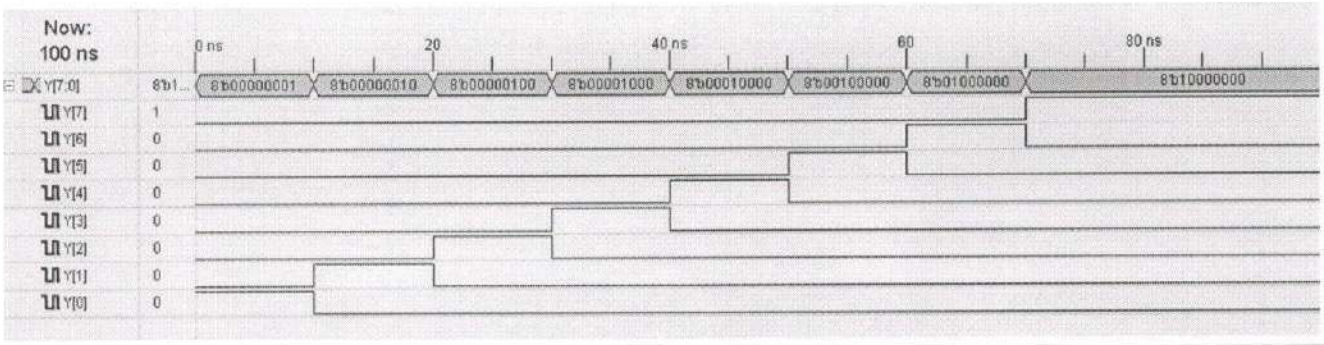
Testbench Output for 3:8 Decoder



Top Module Code for 2-bit comparator

```
module comp_2(a, b, greater, lesser, equal);
output greater, lesser, equal;
input [1:0] a,b;
reg greater, lesser, equal;
always@ (a or b)
begin
if (a > b)
begin
greater=1; lesser=0; equal=0;
end
else if (a < b)
begin
greater=0; lesser=1; equal=0;
end
else
begin
greater=0; lesser=0; equal=1;
end
end
endmodule
```

Testbench Code for 2-bit comparator

```
module comp_2_test;
reg [1:0] a,b;
wire greater, lesser, equal;
comp_2 uut(.a(a), .b(b), .greater(greater), .
lesser(lesser), .equal(equal));
initial
begin
a=0; b=0; #100;
a=5; b=2; #100;
a=2; b=5; #100;
a=5; b=5; #100;
end
initial
begin
#100 $finish;
end
endmodule
```

Truth Table

Inputs				Outputs		
a1	**a0**	**b1**	**b0**	**a > b**	**a < b**	**a = b**
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0

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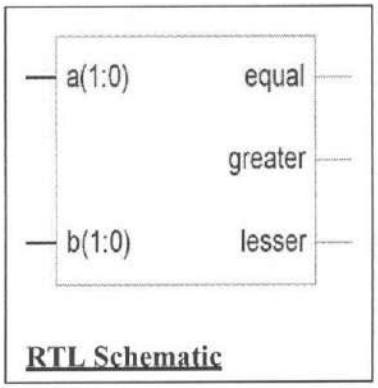
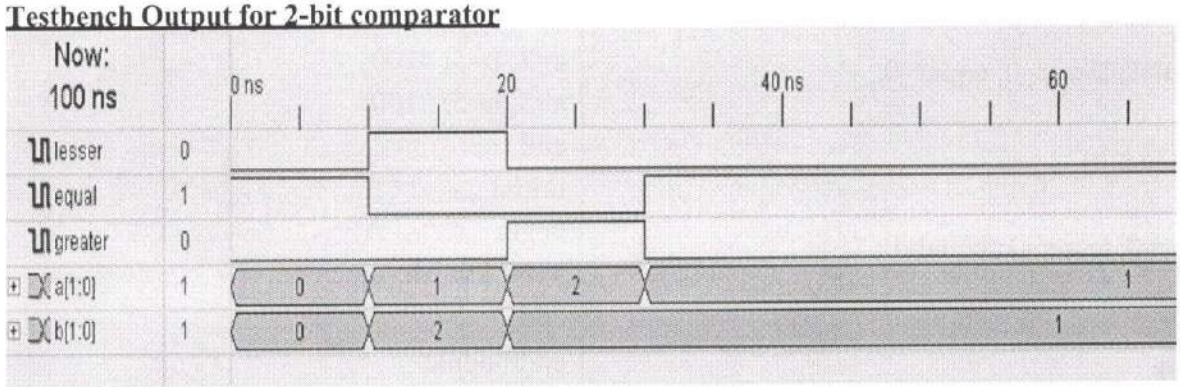
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0



RTL Schematic

Testbench Output for 2-bit comparator



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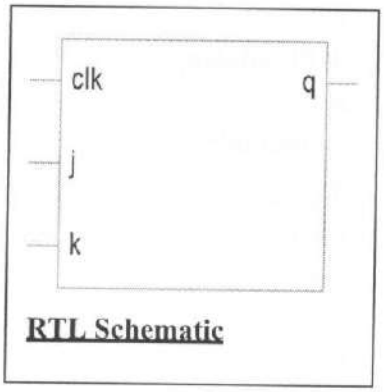
Experiment No: 7

AIM: To realize using Verilog Behavioral description:

Flip-flops: a)JK type b)SR type c)T type and d)D type

Top Module Code for JK Flip Flop

```
module jk_ff (j, k, clk, q);
output q;
input j, k, clk;
reg q;
always@ (posedge clk)
case ({j,k})
2'b00: q<=q;
2'b01: q<=0;
2'b10: q<=1;
2'b11: q<=~q;
endcase
endmodule
```



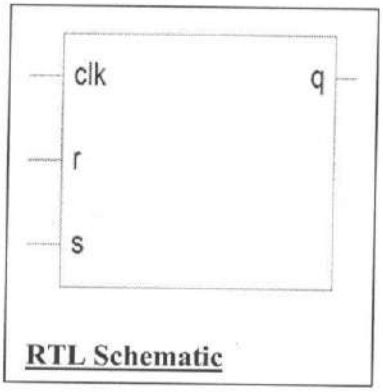
RTL Schematic

Testbench Code for JK Flip Flop

```
module jk_ff_test;
reg j,k,clk;
wire q;
jk_ff uut(.j(j), .k(k), .clk(clk), .q(q));
initial
begin
clk=0;
j=0; k=0; #10;
j=0; k=1; #10;
j=1; k=0; #20;
j=1; k=1; #5;
end
always #5 clk=~clk;
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for SR Flip Flop

```
module sr_ff (s, r, clk, q);
output q;
input s, r, clk;
reg q;
always@ (posedge clk)
case ({s,r})
2'b00: q<=q;
2'b01: q<=0;
2'b10: q<=1;
2'b11: q<=z;
endcase
endmodule
```



RTL Schematic

Testbench Code for SR Flip Flop

```
module sr_ff_test;
reg s,r,clk;
wire q;
sr_ff uut(.s(s), .r(r), .clk(clk), .q(q));
initial
begin
clk=0;
s=0; r=0; #10;
s=0; r=1; #10;
s=1; r=0; #20;
s=1; r=1; #5;
end
always #5 clk=~clk;
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for T Flip Flop

Testbench Code for T Flip Flop

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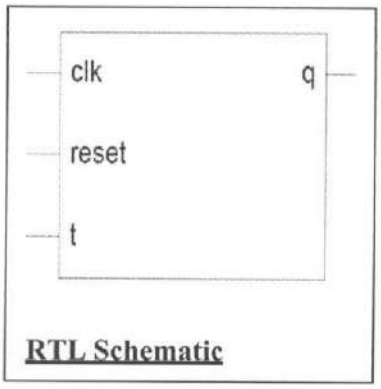
```
module t_ff (t, reset, clk, q);
output q;
input t, reset, clk;
reg q;
always@ (posedge clk)
begin
if (reset)
q<=0;
else
if (t)
q <= ~q;
else
q <= q;
end
endmodule
```

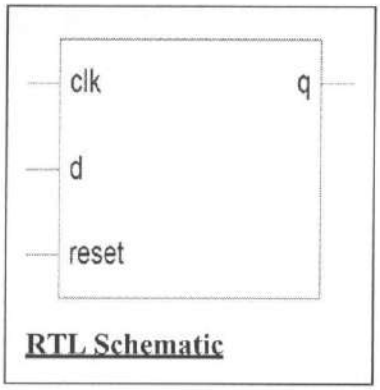


RTL Schematic

```
module t_ff_test;
reg t,reset,clk;
wire q;
t_ff uut(.t(t), .reset(reset), .clk(clk),  .q(q));
always #5 clk = ~clk;
initial
begin
clk=0;
t = 0;
reset = 1;
#10;
t=0; reset=0; #10;
t=1; #100;
end
initial
begin
#100 $finish;
end
endmodule
```

Top Module Code for D Flip Flop

```
module d_ff (d, reset, clk, q);
output q;
input d, reset, clk;
reg q;
always@ (posedge clk)
begin
if (reset)
q<=0;
else
q <= d;
end
endmodule
```



RTL Schematic

Testbench Code for D Flip Flop

```
module d_ff_test;
reg d;
reg reset;
reg clk;
wire q;
d_ff uut (.d(d), .reset(reset), .clk(clk),
.q(q));
initial begin
clk=0;
d = 0;
reset = 1;
#100;
d = 0;
reset = 0;
#100;
d = 1;
end
always #5 clk=~clk;
endmodule
```

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Truth Table for J K Flip Flop

clk	J	K	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	~q --Toggle

Truth Table for SR Flip Flop

clk	S	R	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	X --Indeterminate

Truth Table for T Flip Flop

clk	reset	T	q
↑	0	0	q --No change
↑	0	1	~q --Toggle
↑	1	0	0 --Reset
↑	1	1	0 --Reset

Truth Table for D Flip Flop

clk	reset	D	q
↑	0	0	D -- Input
↑	0	1	D --Input
↑	1	0	0 --Reset
↑	1	1	0 --Reset

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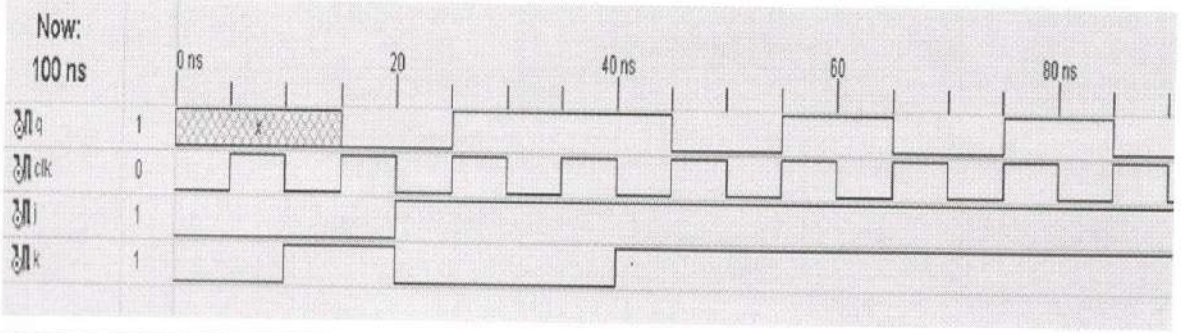
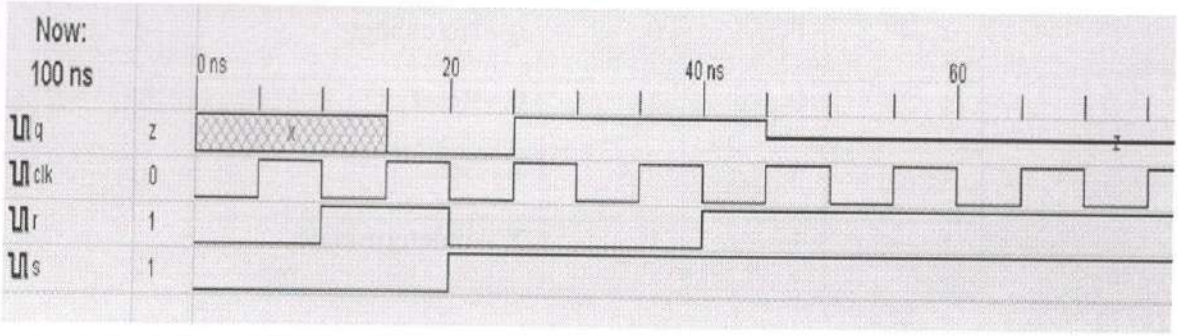
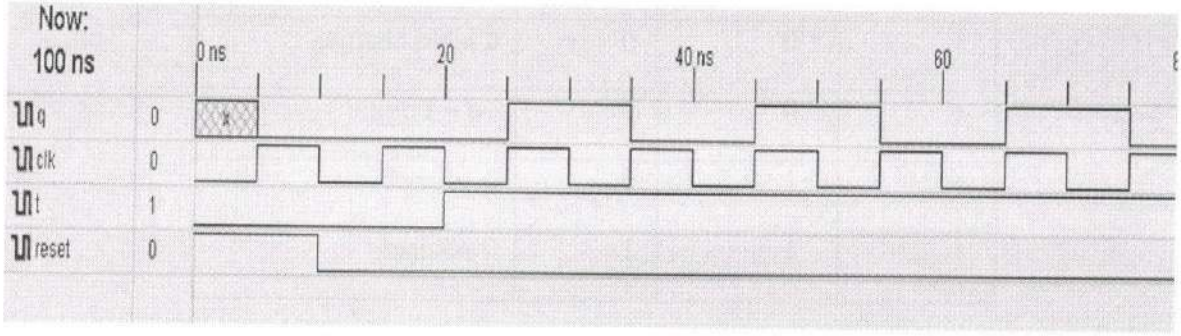
Testbench Output for JK Flip Flop



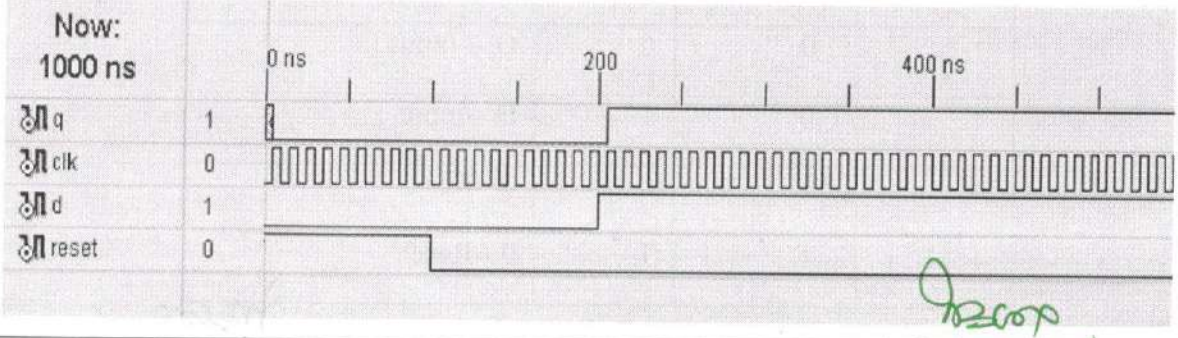
Testbench Output for SR Flip Flop



Testbench Output for T Flip Flop



Testbench Output for D Flip Flop



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Truth Table for J K Flip Flop

clk	J	K	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	~q --Toggle

Truth Table for SR Flip Flop

clk	S	R	q
↑	0	0	q --No change
↑	0	1	0 --Reset
↑	1	0	1 --Set
↑	1	1	X --Indeterminate

Truth Table for T Flip Flop

clk	reset	T	q
↑	0	0	q --No change
↑	0	1	~q --Toggle
↑	1	0	0 --Reset
↑	1	1	0 --Reset

Truth Table for D Flip Flop

clk	reset	D	q
↑	0	0	D -- Input
↑	0	1	D --Input
↑	1	0	0 --Reset
↑	1	1	0 --Reset

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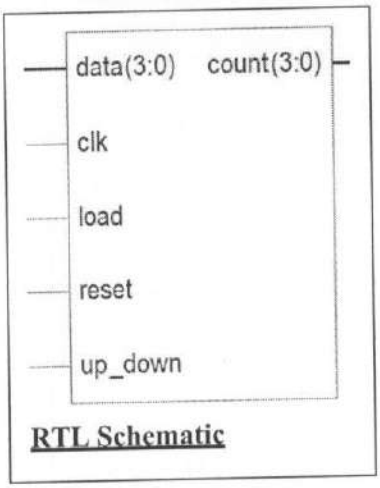
Experiment No: 8

AIM: To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.

Top Module Code for 4-bit Binary Up/Down Counter

```
module binary_counter
(clk,reset,up_down,load,data,count);
input clk,reset,load,up_down;
input [3:0] data;
output [3:0] count;
reg [3:0] count;
always@(posedge clk)
begin
if(reset)
count <= 0;
else if(load)
count <= data;
else if(up_down)
count <= count + 1;
else
count <= count - 1;
end
endmodule
```



RTL Schematic

Testbench Code for 4-bit Binary Up/Down Counter

```
module binary_counter_test;
reg clk;
reg reset;
reg up_down;
reg load;
reg [3:0] data;
wire [3:0] count;
binary_counter uut (.clk(clk), .reset(reset),
.up_down(up_down), .load(load),
.data(data), .count(count));
initial begin clk = 1'b0;
repeat(30)
#3 clk= ~clk;
end
initial begin reset=1'b1;
#7 reset=1'b0;
#35 reset=1'b1;
end
initial begin
#12 load=1'b1;
#5 load=1'b0;
end
initial begin
#5 up_down=1'b1;
#24 up_down=1'b0;
end
initial begin
data=4'b1000;
#14 data=4'b1101;
#2 data=4'b1111;
end
endmodule
```

Top Module Code for 4-bit BCD Up/Down Counter

```
module bcd_counter (clk, reset, count);
input clk, reset;
output [3:0] count;
reg [3:0] count;
```

Testbench Code for 4-bit BCD Up/Down Counter

```
module bcd_counter_tb;
reg clk, reset;
wire [3:0] count;
wire [3:0] tmp;
```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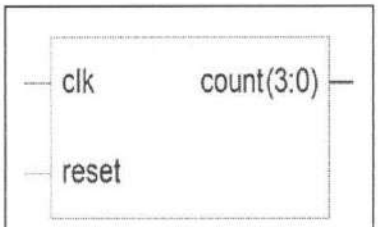
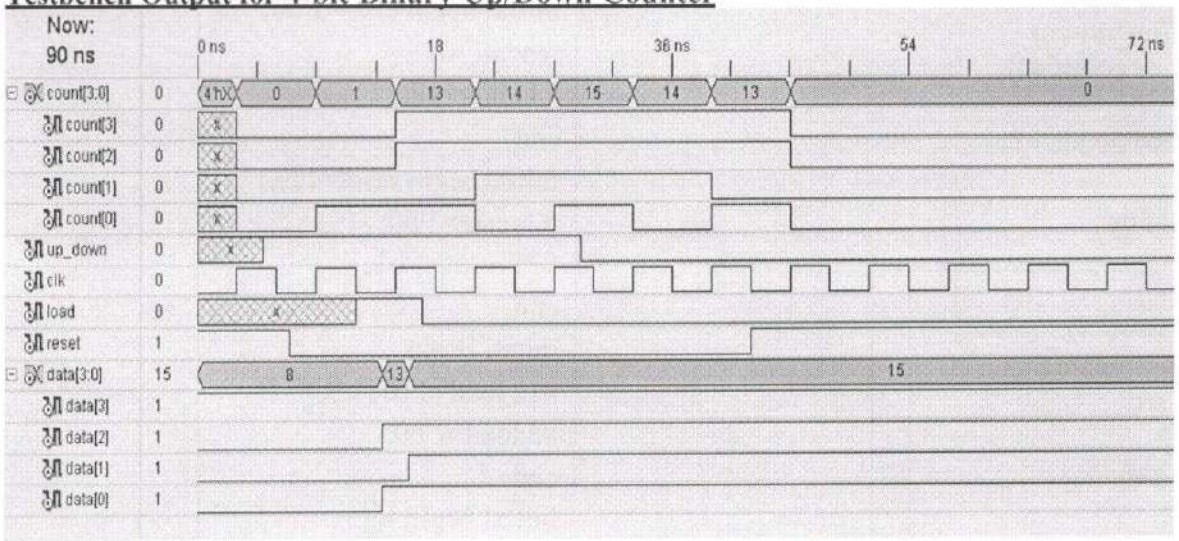
```
reg [3:0] tmp;
always@(posedge clk)
begin
if(reset)
begin
count <= 4'b0000;
tmp <= 4'b0000;
end
else
begin
tmp <= tmp + 1;
if (tmp==4'b1001)
begin
tmp <= 4'b0000;
end
count <= tmp;
end
end
endmodule
```



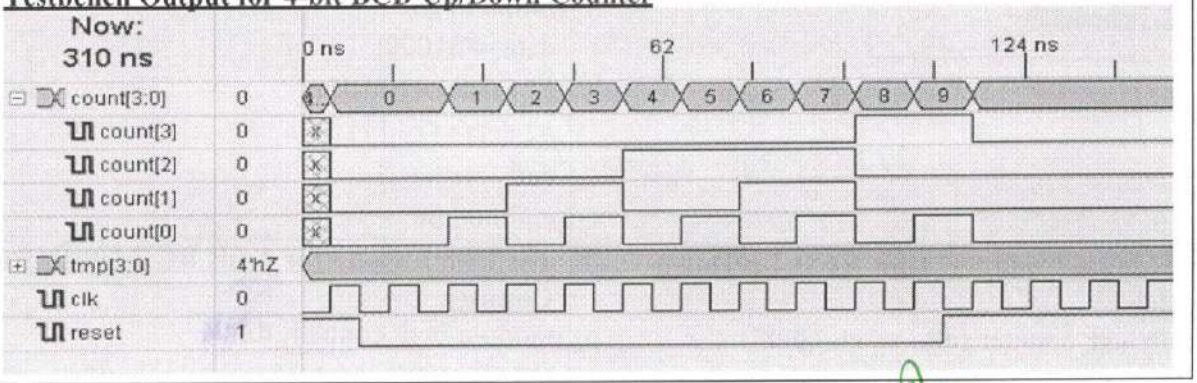
RTL Schematic

```
bcd_counter uut(.clk(clk), .reset(reset),
.count(count));
initial begin
clk = 0;
forever #5 clk = ~ clk;
end
initial begin
reset =1;
#10 reset =0;
#100 reset =1;
#200;
$finish;
end
endmodule
```

Testbench Output for 4-bit Binary Up/Down Counter



Testbench Output for 4-bit BCD Up/Down Counter



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Demonstration Experiments

Experiment No: 1

AIM: Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).

```
module stepper(clk,dir,reset,dout);
input clk, dir, reset;
output [3:0] dout;
reg [3:0] dout;
reg [3:0] shift;
always@ (posedge clk)
begin
clk_div= clk_div+1;
currentstate=nextstate;
end
always@ (posedge clk_div[15])
begin
if (reset==0)
shift=4'b0001;
else if (dir==1)
shift={shift[0], shift[3:1]};
else
shift={shift[2:0], shift[3]};
dout=shift;
end
endmodule
```

UCF File

```
NET "clk" LOC = "p52"
NET "dir" LOC = "p74"
NET "reset" LOC = "p76"
NET "dout<0>" LOC = "p84"
NET "dout<1>" LOC = "p85"
NET "dout<2>" LOC = "p86"
NET "dout<3>" LOC = "p87"
```

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Experiment No: 2

AIM: Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

```
module led_switch (led, switch);
output led;
input switch;
assign led=switch;
endmodule
```

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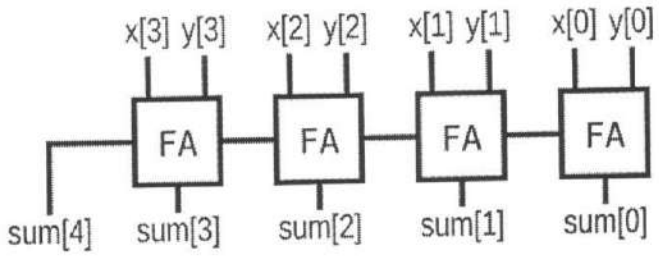
CONTENT BEYOND SYLLABUS

1. Consider the function *f* shown in the Karnaugh map below. Implement this function. **d** is don't-care, which means you may choose to output whatever value is convenient.

x_3x_4 \ x_1x_2	00	01	11	10
00	d	0	d	d
01	0	d	1	0
11	1	1	d	d
10	1	1	0	d

2. Suppose you are designing a circuit to control a cellphone's ringer and vibration motor. Whenever the phone needs to ring from an incoming call (`input` **`ring`**), your circuit must either turn on the ringer (`output` **`ringer`** `= 1`) or the motor (`output` **`motor`** `= 1`), but not both. If the phone is in vibrate mode (`input` **`vibrate_mode`** `= 1`), turn on the motor. Otherwise, turn on the ringer. Try to use only `assign` statements, to see whether you can translate a problem description into a collection of logic gates.

3. Implement the following circuit:



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Vishwothama Nagar, BANTAKAL - 574 115
Udupi District, Karnataka, INDIA

SMVITM

DEPARTMENT OF Electronics and Communication.

Certificate

This is to certify that ~~Mr.~~ / Ms. Nisha

bearing USN 4MW22EC079 has satisfactorily completed the laboratory course Digital System design using verilog lab prescribed by the Visvesvaraya Technological University, Belagavi for the 3rd semester of Bachelor of Engineering in electronics and communication Engineering during the year 2023-24.

27/02/2024

Faculty In-charge

Head of the Department
Dept of E&C Engg.
SMVITM, BANTAKAL - 574 115

19
25

Marks awarded

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INSTITUTE VISION

"To Establish an Excellent, Value-based Higher Educational Hub to Meet the Challenges of Global Competitiveness"

INSTITUTE MISSION

"To impart holistic education with state of the art infrastructural facilities and conducive academic ambience, at affordable costs, leading to the creation of Centers of Excellence with best brains collectively interacting for total personality development and intellectual growth."

DEPARTMENT VISION

To be recognized as a center of eminence in the field of Electronics and Communication Engineering for holistic engineering education and research on current technologies.

DEPARTMENT MISSION

1. Impart quality engineering education with ethics to students and transform them into leaders in technology, innovation and research.
2. Provide a platform and academic atmosphere that will ensure the transfer of knowledge and skills to the students.
3. Promote the overall personality development of the students through activities that have high credibility and social impact.

PROGRAM EDUCATIONAL OBJECTIVES

The graduate of Electronics and Communication Engineering should be able to

PEO-1 Exhibit essential knowledge of applied sciences mathematical modelling, logical interpretation and visual realization to resolve real-time problems in the field of electronics and communication engineering.

PEO-2 Work productivity as an electronics and communication engineer, including supportive and leadership roles on multidisciplinary teams.

PEO-3 Inculcate effective communication skills to excel in professional growth.

PEO-4 Take part in lifelong learning in pace with the advancing technological society.

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EVALUATION SCHEME

Sl. No.	Description	Marks	
		Maximum	Alloted
1.	Continuous Internal Evaluation	15	15
2	Internal Assessment	10	04
	TOTAL	25	19

Student Signature

07/02/2024

Faculty Signature

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COURSE OUTCOMES

This course will enable the students to:

- To impart the concepts of simplifying the Boolean expression using k-map techniques and Quine-Mc cluskey minimization techniques.
- To impart the concepts of designing and analysing combinational logic circuits.
- To impart design methods and analysis of sequencing logic circuits.
- To impart the concepts of Verilog-HDL dataflow and behavioural models for the design of digital systems.

PROGRAM OUTCOMES

PO 1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2 **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4 **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6 **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7 **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10 **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1: Understand the concepts of electronics and communication engineering and its applications in the fields of signal processing, control system, VLSI design, networking and communication.

PSO2: Apply the domain specific knowledge to design, analyse, synthesize and validate real time problems in electronics and communication engineering.

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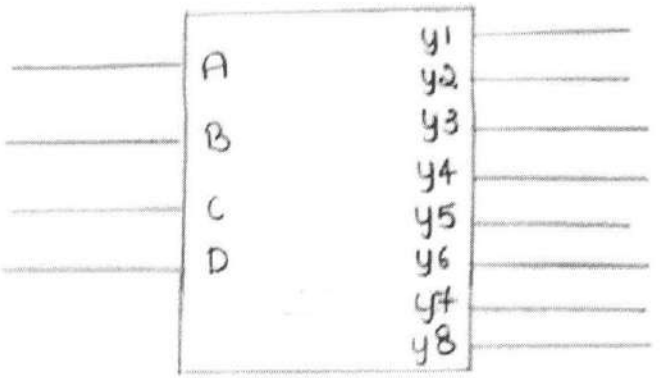
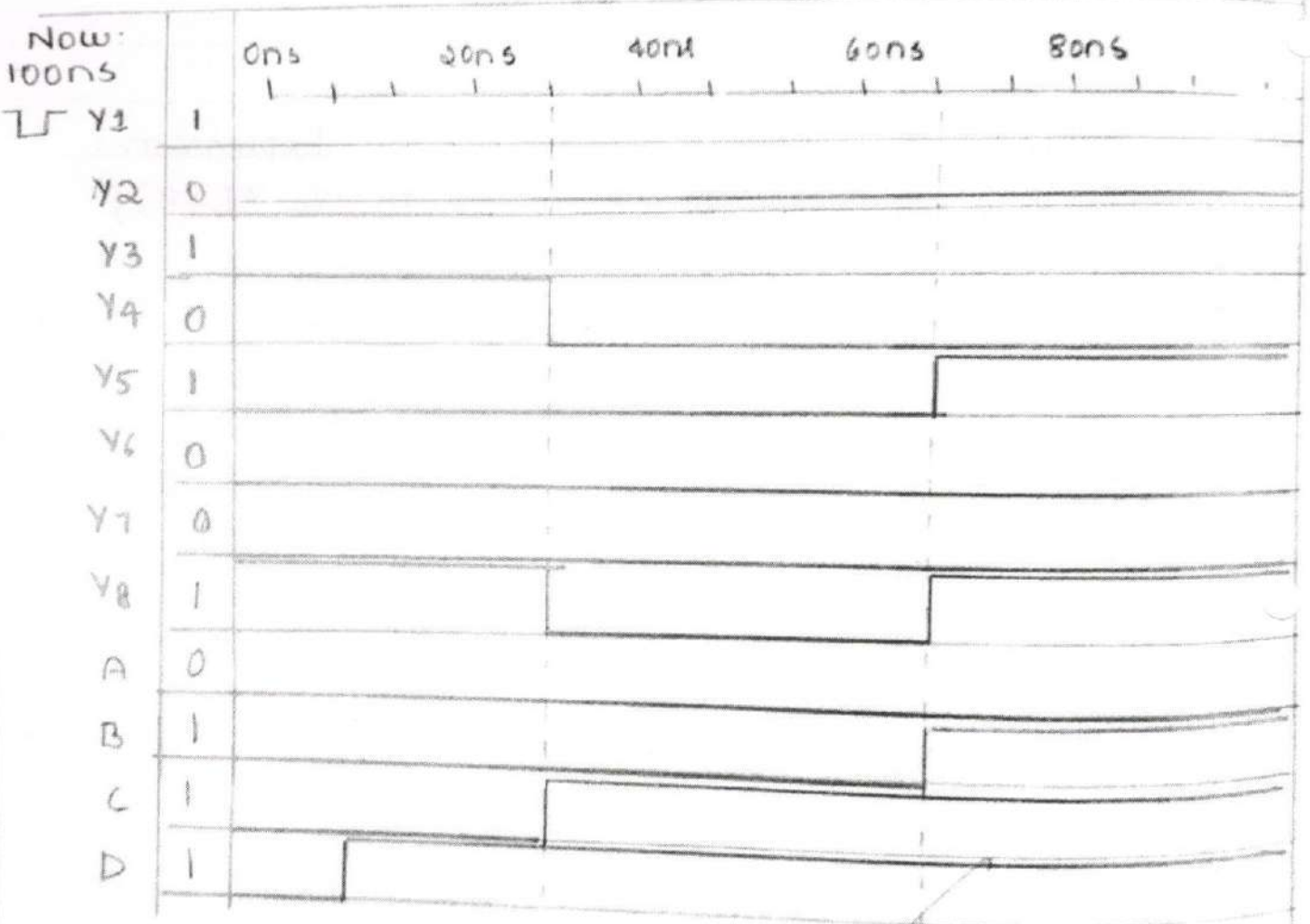
RTL Schematic



Testbench output:



$Y1 = A'B' + AB + A'B$.

$= A'(B'+B) + AB$

$= A' + AB$

$= A' \cdot 1 + AB$

$= A' + B(A'+A)$

$= A' + B(A'+A) = A' + B$ //.

$Y2 = (A+B)(A+B')$

$= AA + AB' + AB + BB'$

$= A + A(B'+B)$

$= A + A(1)$

$= A$

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Experiment No. 1

Date 20/11/23

Aim: To simplify the given Boolean expressions and realize using Verilog program.

$Y1 = A'B' + AB + A'B$.

$Y2 = (A+B)(A+B')$

$Y3 = A'B + AB' + A'B' + AB$

$Y4 = AB' + BC' + AC'$

$Y5 = A'BC + AC$

$Y6 = AB + ACCD + CD')$

$Y7 = (BC' + A'D)(AB' + CD')$

$Y8 = A'BC + AB'C' + A'B'C' + ABC$

Top Module Program for Boolean Expression:

```
module bool(A,B,C,D,Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8);
input A,B,C,D;
output Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
assign Y1 = ~A|B;
assign Y2=A;
assign Y3=1;
assign Y4=(A&(~B))|((~A)&(~C));
assign Y5= C&(A|B);
assign Y6 = A&(B|C);
assign Y7=0;
assign Y8=(B&C)|((~B)&(~C));
endmodule
```

TestBench code for Boolean Expression

```
module bool_test;
reg A,B,C,D;
wire Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8;
```


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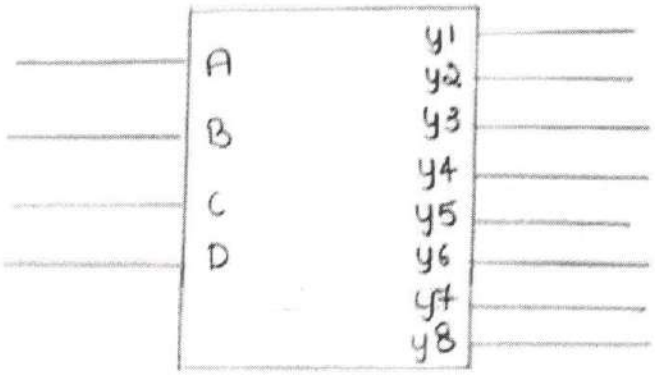
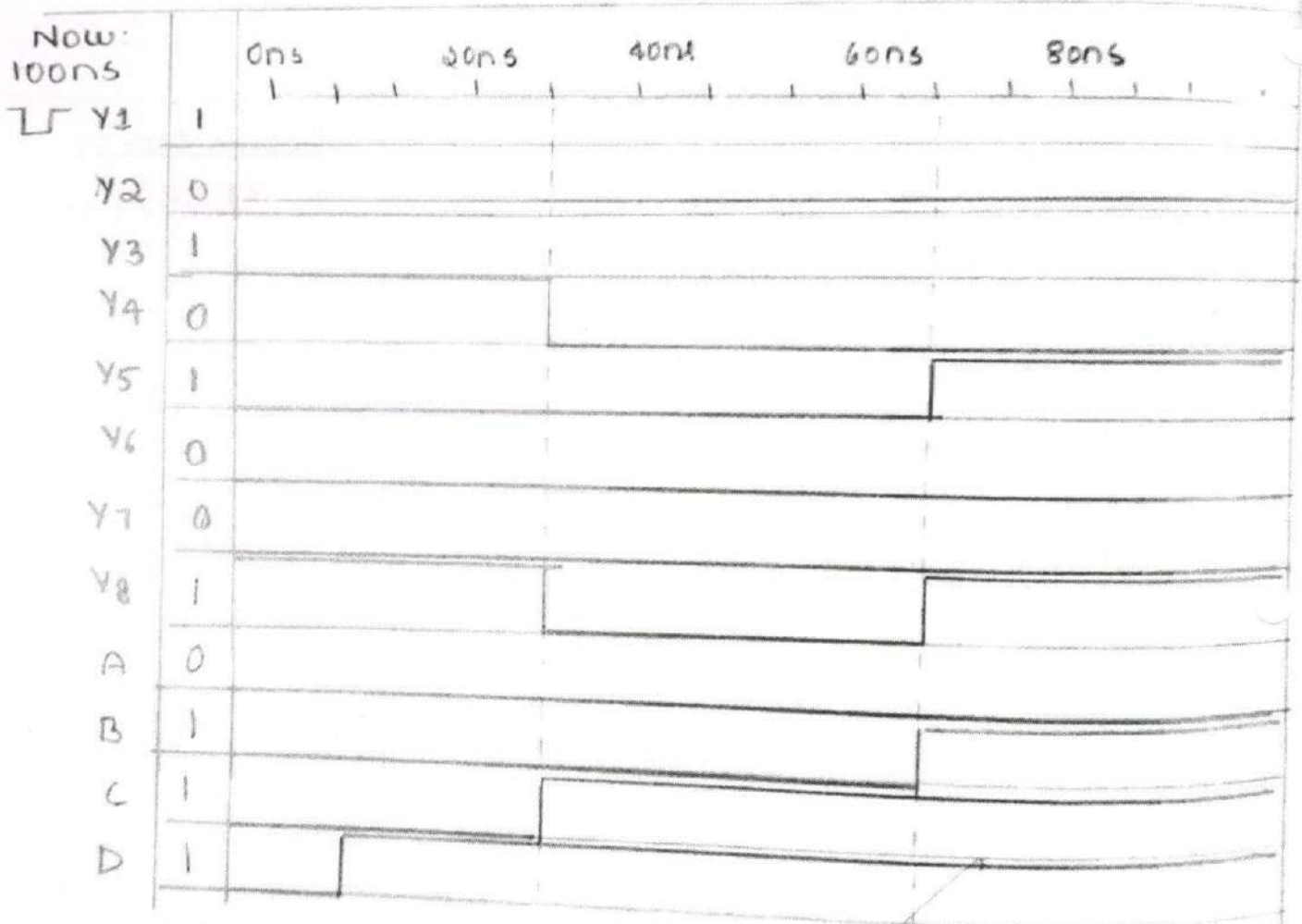
RTL Schematic



Testbench output:



$Y1 = A'B' + AB + A'B$.

$= A'(B'+B) + AB$.

$= A' + AB$

$= A' \cdot 1 + AB$

$= A' + B(A'+A)$

$= A' + B(A'+A) = A' + B$ //.

$Y2 = (A+B)(A+B')$

$= AA + AB' + AB + BB'$

$= A + A(B'+B)$

$= A + A(1)$

$= A$

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Experiment No.

Date

```
bool uut (.A(A), .B(B), .C(C), .D(D), .Y1(Y1), .Y2(Y2), .Y3(Y3), .Y4
(Y4), .Y5(Y5), .Y6(Y6), .Y7(Y7), .Y8(Y8));
initial
begin
A=0; B=0; C=0; D=0;
end
always
begin
#10 D=!D;
#20 C=!C;
#40 B=!B;
#80 A=!A;
end
initial
begin
#200 $finish;
end
endmodule
```


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~~Truth Table~~ :

$Y3 = A'B + BB' + A'B' + AB$

$= A'(B+B') + A(B'+B)$

$= A'(1) + A(1) = A' + A$

$= \underline{1}$

$Y4 = AB' + B'C' + A'C'$

$= AB' + A'C' + B'C'(A+A')$

$= AB' + A'C' + AB'C' + A'BC'$

$= AB'(1+C') + A'C'(1+B') + A'B'C'$

$= AB'(1+C') + A'C'$

$= \underline{AB' + A'C'}$

$Y5 = A'BC + AC$

$= A'BC + AC(B+B')$

$= A'BC + ABC + AB'C$

$= BC(A'+A) + AB'C$

$= BC + AB'C$

$= C(B + AB')$

$= C(B+A) = \underline{BC + AC}$

$Y6 = AB + AC(D+CD')$

$= AB + ACD + ACD'$

$= AB + AC(D+D')$

$= AB + AC = \underline{A(B+C)}$

$Y7 = (BC' + A'D)(AB' + CD')$

$= BC' \cdot AB' + B'C' \cdot CD' + A'D \cdot AB' + A'D \cdot CD'$

$= 0$

$Y8 = A'BC + AB'C' + A'B'C' + ABC$

$= A'BC + B'C'(A+A') + ABC$

$= A'BC + B'C' + ABC$

$= BC(A'+A) + B'C'$

$Y8 = \underline{BC + B'C'}$

Truth Table :

Inputs				Outputs							
A	B	C	D	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	1	0	1	1	0	0	0	1
0	0	0	1	1	0	1	1	0	0	0	1
0	0	1	0	1	0	1	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	0
0	1	0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	1	0	1	0	1	0	0	1
0	1	1	1	0	1	1	0	1	0	0	1
1	0	0	0	1	0	1	1	0	0	0	1
1	0	0	1	0	1	1	1	0	0	0	1
1	0	1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	1	1	0	0	0	0	0
1	1	0	0	1	0	1	1	0	0	0	0
1	1	0	1	0	1	1	1	0	0	0	0
1	1	1	0	1	0	1	0	0	0	0	0
1	1	1	1	0	1	1	0	0	0	0	0

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SMVITM

MINUTES OF MEETING

Date: November 3, 2023
Time: 11:00 AM – 12:00 Noon
Venue: VLSI Lab (ECE Block)
Agenda:

1. Department Highlights
2. Result Analysis
3. PO Attainment of 2019-23 Batch
4. Any other academic matter

Attendance: As per the List Attached

No.	Discussion and Action to be taken	Responsibility	Target Date
1	Dr. Guruprasad welcomed all the PAC members to the meeting.	-	-
2	Ms. Sowmya Bhat briefed the PAC members, the highlights and accomplishments of faculties and students of the ECE department for the AY- 2022-23, the result analysis of 6th and 8th semester end examinations. The 2nd and 4th semester results were not yet declared.	-	-
3	PO-PSO attainment of 2019-23 batch was displayed. In all the POs and PSOs the attainment was above 70% of the maximum.	Course Faculty Members	Ongoing
4	• The present best practices to improve the teaching learning process were presented. • However, the further suggestions for the better performance of students in placement drives were discussed 1. Training sessions on Java and JavaScript, to help the students crack the interview questions in IT company recruitment drives. 2. Introductory sessions on GitHub. 3. Peer to Peer sessions on Analog and Digital Electronics concepts during placement hour for final year students.	Faculty Members and students	Ongoing
5	Dr. Guruprasad thanked all the members for participating in the meeting and sharing their valuable views.	-	-

Enclosure: Attendance sheet

03/11/2023
Ms. Sowmya Bhat
Program Coordinator

3/11/23
Dr. Guruprasad
I/c HOD-ECE

Copy to:
1. All PAC members
2. Principal
3. IQAC

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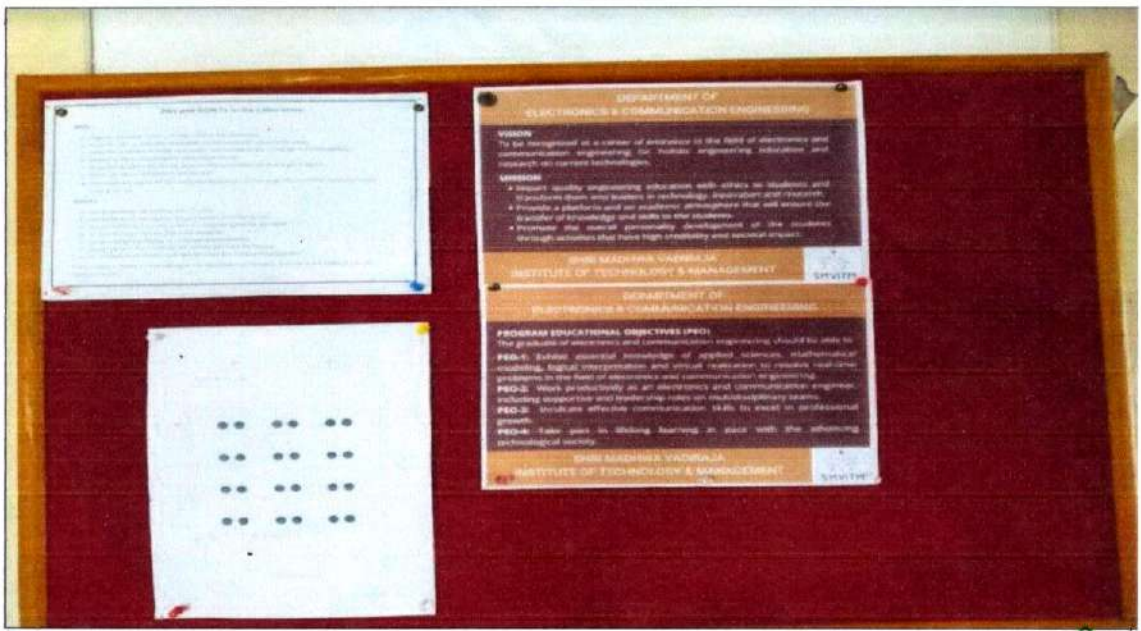
Dissemination of PEOs, POs and PSOs

PEOs displayed in Department of Electronics & Communication Engineering Library
Latitude: 13.254544^0
Longitude: 74.785569^0



PEOs displayed in Department of Electronics & Communication Engineering Project Lab Notice Board
Latitude: 13.254703^0
Longitude: 74.785535^0

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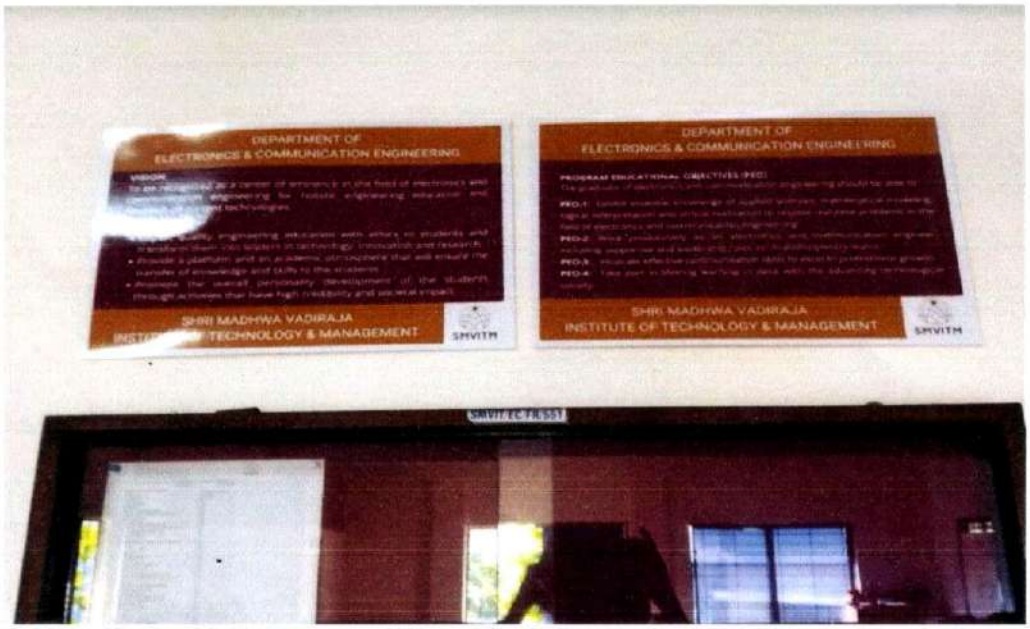
PEOs displayed in Department of Electronics & Communication Notice Board near entrance
Latitude: 13.254658^0
Longitude: 74.78571^0



PEOs displayed in Department of Electronics & Communication Engineering Faculty Cabin
Latitude: 13.254458^0
Longitude: 74.785578^0

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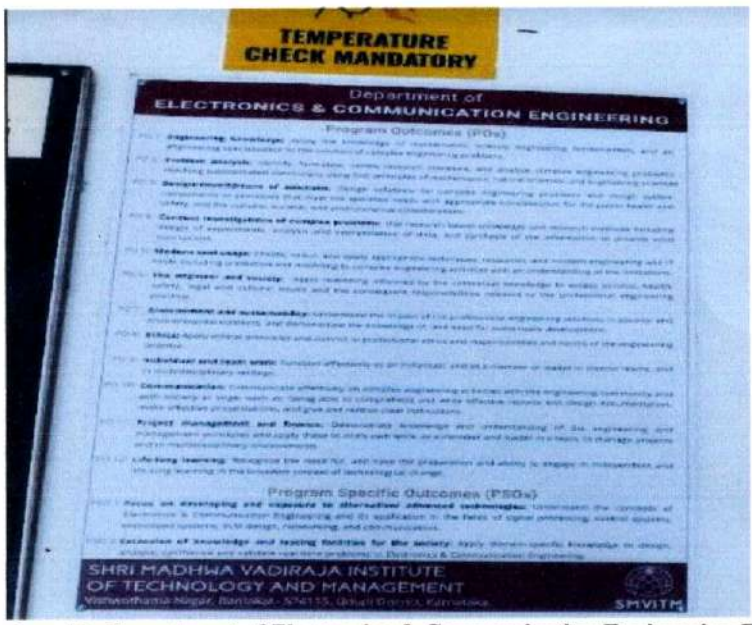
PEOs displayed in Department of Electronics & Communication Engineering Corridor Notice Board
Latitude: 13.254703^0
Longitude: 74.785575^0



POs displayed in Department of Electronics & Communication Engineering Entrance
Latitude: 13.254688^0
Longitude: 74.785576^0

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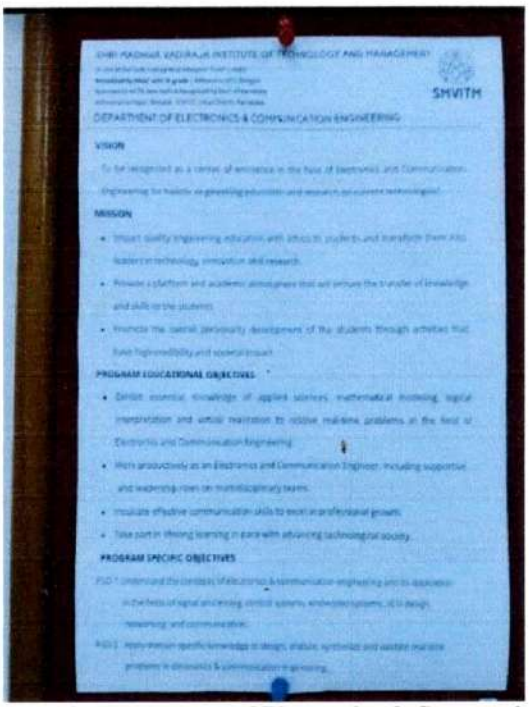

PEOs and PSOs displayed in Department of Electronics & Communication HOD's Cabin
Latitude: 13.254703^0
Longitude: 74.785575^0

PEOs, POs and PSOs displayed in Department of Electronics & Communication Engineering Notice Board
Latitude: 13.254596^0
Longitude: 74.785478^0

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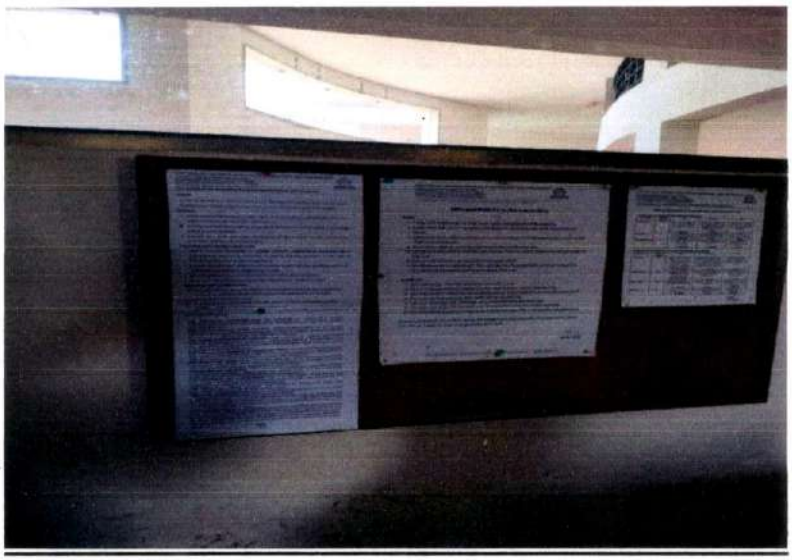

PEOs, POs and PSOs displayed in Department of Electronics & Communication Engineering Digital Signal Processing Laboratory Notice Board
Latitude: 13.254596^0
Longitude: 74.785478^0

PEOs, POs and PSOs displayed in Department of Electronics & Communication Engineering Faculty Cabin Notice Board
Latitude: 13.254596^0
Longitude: 74.785478^0

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PEOs displayed in Department of Electronics & Communication Engineering Classroom
Latitude: 13.254596^0
Longitude: 74.785674^0

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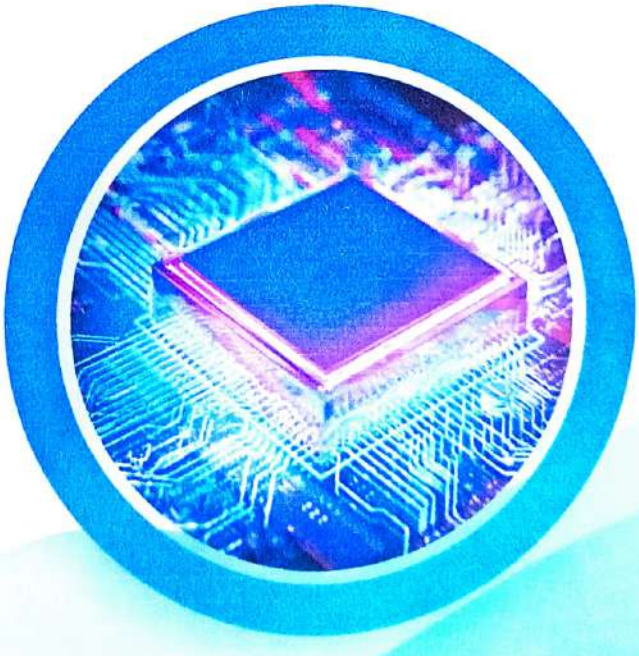
TECH TARANGA

A Departmental Newsletter
from
Electronics and Communication Engineering



VOL 8 | ISSUE 2 | YEAR 2022-2023

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HOD's MESSAGE

Greetings to all the readers of ★★ *Tech Taranga* ★★

We cordially invite you all to read this issue of the Electronics and Communication Engineering Department Newsletter. The launch of **"*Tech Taranga*"** our biannual newsletter fills us with excitement. This newsletter will provide a succinct rundown of the department's successes and activities. We have always used the electronic newsletter ***Tech Taranga*** to interact with our alumni, professors, students, and business partners. Additionally, by emphasizing diverse activities including placement, alumni, institutional club activities, student and staff successes, it updates readers on the most recent departmental happenings. We expect more efforts and accomplishments to support the department's continued ascent to excellence. We would like to convey our appreciation for the teaching staff, support staff, and our beloved students for their consistent support.

Principal
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Dr. Gurupraxad

ABOUT DEPARTMENT

Electronics today stands at the forefront of the rapidly expanding horizon of Science and Technology. The Department of Electronics and Communication Engineering in SMVITM was established in the year 2010, initially offering an undergraduate program with an intake of 60 students per year. The intake was increased to 120 in the academic year 2012-13. The department has well-qualified faculty members – highly motivated in teaching and guiding the students in exploring newer avenues of electronics and communication.

The department is intent on creative and technologically advanced skill transfer to the students through teaching, mentoring and counseling. It regularly organizes seminars, symposiums, workshops and invited talks by eminent faculty from reputed institutions and industry experts, to keep the students abreast of the latest technological developments in related fields. The services of some academicians of high repute have been utilized by the department with the objective of supplementing teaching, mentoring and guiding the students as well as faculty members.

The department has its own library comprising of over 200 text books and technical magazines for quick reference. To nurture creative ideas and provide hands-on training to the students, the department has set up an Innovation/Project laboratory with state-of-the-art equipment and latest versions of software tools, in addition to the regular laboratories.

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OUR VISION

"To be recognized as a center of eminence in the field of Electronics and Communication Engineering focusing on holistic engineering education and current technologies".

OUR MISSION

- Impart quality engineering education with ethics to students and transform them into leaders in technology, innovation and research.
- Provide a platform and academic atmosphere that will ensure the transfer of knowledge and skills to the students.
- Promote the overall personality development of the students through activities that have high credibility and societal impact.

PROGRAM EDUCATIONAL OBJECTIVES

The graduate of Electronics & Communication Engineering should be able to:

- Exhibit essential knowledge of applied sciences, mathematical modelling, logical interpretation and virtual realization to resolve real-time problems in the field of Electronics and Communication Engineering.
- Work productively as an Electronics and Communication Engineer, including supportive and leadership roles on multidisciplinary teams.
- Inculcate effective communication skills to excel in professional growth.
- Take part in lifelong learning in pace with the advancing technological society.

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PROGRAM OUTCOMES

Graduates of the Electronics and Communication Engineering program are able to:

PO-1	Engineering Knowledge	Develop skills to solve engineering problems by using mathematical, scientific and engineering knowledge.
PO-2	Problem Analysis	Recognize, define, conduct literature survey, examine complex engineering problems and draw conclusions using the principles of mathematics, science and engineering
PO-3	Design/Development of Solutions:	Express ideas, devise implementation strategies, plan execution and synthesize solutions, which are favorable for aspects of public health and safety as well as for cultural, societal and environmental conditions
PO-4	Conduct investigations of complex problems	Investigate complex problems by conducting experiments and validate the results
PO-5	Modern Tool Usage	Employ necessary techniques using modern hardware and software tools for engineering applications
PO-6	The Engineer and Society	Reckon and address the societal, health, safety, legal and cultural issues and adopt responsibilities adhering to professional engineering practice.
PO-7	Environment and Sustainability	Estimate and attend to environmental safety issues by means of engineering practice.
PO-8	Ethics	Understand and apply professional ethics for issues relevant to the engineering practices
PO-9	Individual and Team Work	Work as a member of a multidisciplinary project or research teams and have an understanding of leadership in teams and organizations.
PO-10	Communication	Produce engineering reports and express the ideologies effectively.
PO-11	Project Management and Finance	Apply managerial skill in handling projects as a member and leader of a multi-discipline team
PO-12	Life-long Learning	Evolve through lifelong learning process to keep one updated in technological changes.

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PROGRAM SPECIFIC OUTCOMES

Graduates of Electronics & Communication Engineering will be able to:

- Focus on developing and exposure to alternative/ advanced technologies: Understand the concepts of Electronics & Communication Engineering and its application in the fields of signal processing, control systems, embedded systems, VLSI design, networking, and communication.

- Extension of knowledge and testing facilities for the society: Apply domain-specific knowledge to design, analyse, synthesise and validate real-time problems in Electronics & Communication Engineering.

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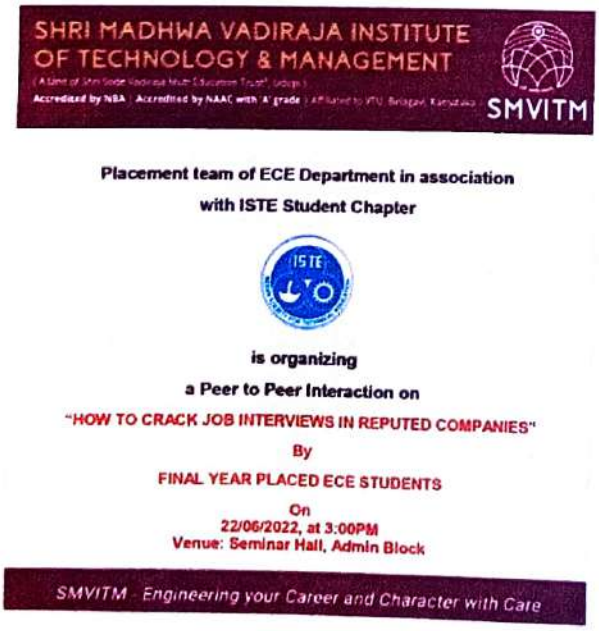
DEPARTMENTAL ACTIVITIES

1. **"Peer to Peer Interaction: How To Crack The Job interviews in Reputed Companies"**

Placement Team of the ECE Dept. in association with the ISTE student chapter has organized "Peer to Peer Interaction: How to Crack the Jobs in Reputed Companies". This interaction was held on 2/06/2022, from 3pm to 4.30pm at the Seminar Hall, Admin Block, SMVITM. The resource person for this interaction was 8th semester ECE placed students. Around 30 students from 6th semester ECE participated and interacted with 15 placed ECE final year students.



The interaction began with the motivational speech by Mr. Sachin Prabhu, Sr. Assistant Professor, Dept. of ECE and inspired the students to start preparing for the placements. There was an open discussion about the preparation for interview, focusing areas and technical background. The placed students also shared their experience regarding their interview
Process and gave proper directions regarding placements. Ms. Niharika, 8th semester ECE student welcomed the resource person and audience. Mr.Chetan, ISTE coordinator and Ms. Yogeshwary B H, Department Placement coordinator has coordinated the interaction.

2. **Bridge course on Aurdino- Ideathon and Hackathon**

Electronics & Communication Engg.. Department in association with ISTE student Chapter has organized the bridge course on Aurdino- Ideathon and Hackathon Phase I training held from 10th October 2022 to 14th October 2022 and Phase II training from 17th October 2022 to 19th October 2022.Training was given by ECE dept. faculties and final year students. At the end of the bridge course Ideathon and Hackathon competitions were conducted and best presenter was recognized and awarded with cash prize.

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3. Invited Talk on "Problem Solving and Idea Generation"

Department of Electronics and Communication Engineering in association with ISTE Studentb Chapter and IIC has organized an invited talk on the topic "Problem Solving and Idea Generation" on 31-10-2022 at 3:00p.m in EC010 (ECE Department). Mr. David Saldanha, CEO at Aion Health Solutions Pvt. Ltd. Bengaluru was the resource person.

The talk started with the first significant step of Problem Solving and Idea Generation is formulating the problem statement. Further, to find a solution to the identified problem there are different ways to be followed. Some important steps are listening, observing and writing down the ideas. He has stressed upon each of these topics separately by giving real time examples and illustrations. Also he has given the examples of Larry Page and others who have made the impossible things possible by looking at things differently. He gave insights on sharing one's own idea with the team to get the motivation and new perspective to solve the problem. He shared his own life story to motivate the students and concluded the talk with the message to convert your novel idea into a final product, in-spite of all the difficulties you face in the middle of the work. Ankita Bhat, 5th semester, ECE was the Master of the Ceremony and Arun J.K, secretary, ISTE Student Chapter proposed the vote of thanks. Dr. Sachin Bhat, HoD, Dept. of ECE, Mr. Sandesh Kumar, IIC Dept. Coordinator, and Ms. Chandana, ISTE Dept. Coordinator, were present during the event. The event was coordinated by Ms. Chandana, ISTE Dept. Coordinator with the support of Mr. Chetan R, Secretary/Treasurer ISTE.

4. Peer Learning Session on "Internship Opportunities in Startups"

Department of Electronics and Communication Engineering in association with ISTE Student Chapter and IIC had organized a Peer Learning Session on 22-11-2022 at 12:00p.m in EC012
(ECE Department). The Final Year Students from the ECE Department were the resource persons. Ms. Sameeksha P U started her talk by sharing the experience about her internship in VI Solutions Bangalore. She briefed about NI Lab View software and application of the same. At the end of her session, she showed the project that she worked on during her internship. The session was continued by Ms. Shreya Upendra Nayak, who did her internship from BEL, in Machilipatnam. She shared her experience of 4 weeks of internship. She discussed about the YOLO algorithm, Animal Detection and Number Plate Detection on which she worked during her internship period. Later the session was taken over by Ms. Akshatha Renjal who is currently undergoing a research internship. She talked about the challenges faced by her during the collection of real-time data (number plate detection of a vehicle which has undergone an accident) and processing of the collected data. She told about the importance of survey and how the

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communication among the team members is important in completing any given task.
Mr. Adithya Prakash, 5th semester, ECE and active member of ISTE Student Chapter was the Master of the Ceremony. Dr. Sachin S Bhat, HoD, Department of Electronics and Communication Engineering was present during the event. The event was coordinated by Ms. Chandana, ISTE Department Coordinator with the support of Mr. Chetan R, Secretary of ISTE.

5. TECH TALK 1.0

Technocrators Club of Electronics and Communication Department in association with ISTE
Students Chapter has conducted the TECH TALK 1.0 event on 15/12/2022 at 2:00PM in the college premises. Mr. Ranjith Bhat, Sr. Asst. Professor, ECE Dept. and Mr. Sunil Haldankar, Sr. Asst. Professor, CV Dept. were the judges. In the competition students spoke on the topics IOT in Healthcare, Communication technology, Metaverse, Natural Language Processing, Green building, Cracks in concrete, Electric Vehicles, Nanomaterial. The program was compeered by Ms. Shreya Upendra Nayak, coordinator of Technocraters club. Mr. Shreepathi and Mr. Shrinidhi, final year ECE students were volunteers for the event. Mr. Chetan R Institutional Coordinator ISTE Faculty Chapter, Ms. Jayashree M coordinator of Techno Crators , Mr. Nagaraja Rao and Ms.Lahari Vaidya were present in the event . Adithya S Bhat, final year student proposed the vote of thanks. Mr. Ashwin kumar G Rao, first year, CSE Dept. and Ms. Ankitha Shet, third year, ECE Dept. have shared the first prize.

6. Hands on session on "Learn to repair & troubleshoot electronics"

Department of Electronics and Communication Engineering in association with ISTE Student Chapter has organized a hands-on session on "Learn to repair & troubleshoot electronics" on 17-12-2022 at 10:00a.m in Analog Electronics Lab (ECE Department). Mr. Madhusudhan Thanthry P. N, Foreman and Mr.Sandeep K.R, Sr. Lab Instructor, Department of ECE were the resource persons. The session started with a small introduction to the power supply and different components involved in the power

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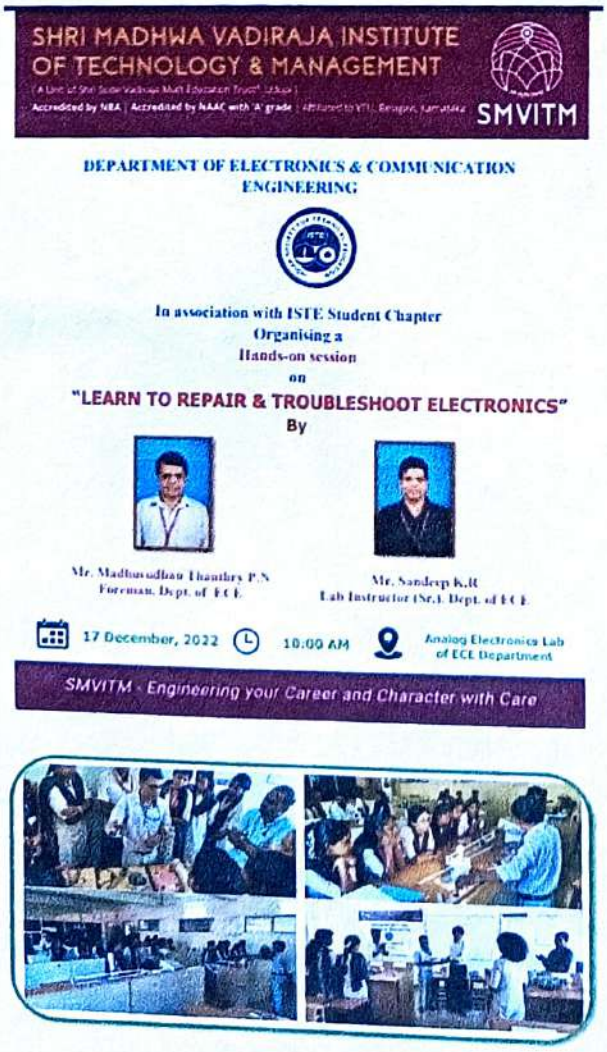
supply. Students were divided into groups and each group of students explored the concepts through hands-on experience. In the first half of the session, students were taught soldering, how to make the connections using wires and switches, how to light a bulb and to connect relay circuits. In the second part of the session, the participants got an exposure to know more about home appliances such as mixer, iron box, TV, lamp, stabilizer, electric water heater immersion coil etc. Chaitanya Anant Nilekani, 3rd semester, ECE was the Master of the Ceremony. Dr. Sachin Bhat, HoD, Department of Electronics and Communication, was present during the event. The event was coordinated by Ms. Chandana, ISTE Department Coordinator with the support of Mr. Chetan R, Secretary/Treasurer ISTE.



7. CIRCUIT DEBUG 1.0

TechnoCrators Club of Electronics and Communication Department in association with ISTE Students Chapter has conducted the CIRCUIT DEBUG 1.0 event on 22/12/2022 at 11:00AM in the ECE Dept. Mr. Sandesh Kumar, Sr. Asst. Professor, ECE Dept. and Ms. Vijayalatha Devadiga, Sr. Asst.Professor, ECE Dept. were the judges. The first round was the MCQ round followed by the Circuit Rig Up and finally the Circuit Debug Round.

The program was compeered by Ms. Shreya Upendra Nayak coordinator of Techno Crators club and Ms. Sukhitha K S,7th Semester,ECE, Mr. Deepak Adhikari and Mr. Lloyd Winston Pinto,5th Semester ECE students were volunteers for the event. Mr. Chetan R Institutional Coordinator ISTE Faculty Chapter, Ms. Jayashree M coordinator of Techno Crators,were present. Mr. Tanmay Kalkur and Mr. Swasthik of 5th sem ECE, secured the first prize in the circuit debug.

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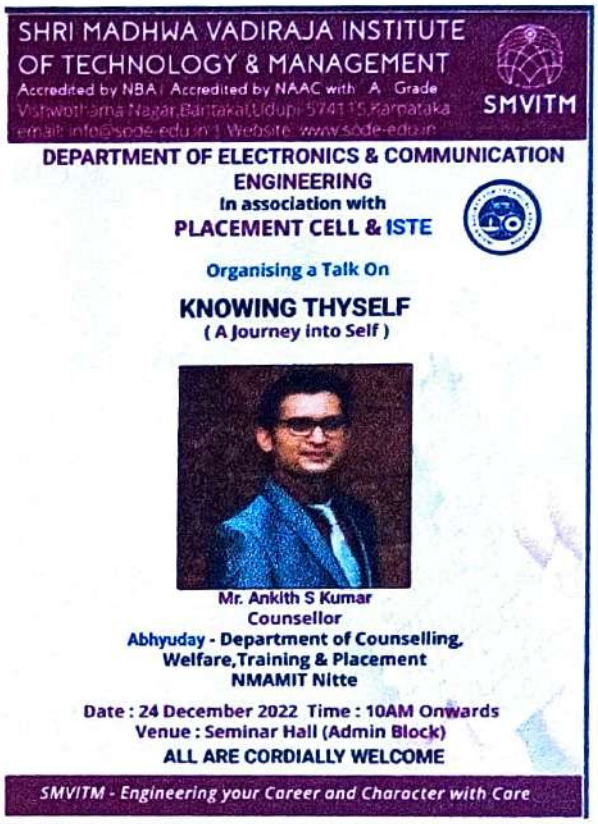
8. Knowing Thyself- Journey into Self

Department of Electronics and Communication in association with placement cell & ISTE student chapter organized a talk on " Knowing Thyself- A journey into self" on 24/12/2022 at 10am onwards in Seminar Hall, Admin Block, SMVITM for Final year students of all branches & pre final year students of ECE. The resource person was Mr. Ankith S Kumar, Counsellor, Abhyday- Department of Counselling, Welfare, Training & Placement, NMAMIT, NITTE.

The Agenda of talk covered topics like mind health, brain space that's been utilized, knowing about inner self of an individual when time spent all alone. It also focused on topics like distortion that is present in outside world, what to & how to focus on things which are important. Mr. Ankith also stressed on topics like positive attitude & having one, how it makes a difference; about values & ethics. He also spoke about ideal self, real self & societal self, human behaviour in general & also discussed about how to deal with challenges that comes ahead in life. The session was activity based learning; it was truly inspiring & motivational session to students. Ms.Shreya Upendra Nayak, Ms. Sukitha, 8th sem ECE students hosted & welcomed the session & Ms. Athmika,5th sem ECE delivered vote of thanks.

ISTE Coordinator Mr. Chethan, Placement coordinators Ms. Yogeshwari & Ms.Lahari organized the program & Session was graced by HoD's of ECE, Civil & accompanied by Senior Faculties, Staffs & Students of SMVITM.



9. Workshop on "Python & GUI"

The Department of ECE in association with ISTE student chapter has organized two days workshop on "Python & GUI" on 10th and 11th January 2023 for the benefit of the ECE students. Mr. Mahesh Deginal, Managing director of Karunadu Technologies was the resource person for the workshop.

In this workshop, the students have learnt about python which is a trending high level

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programming language and can be used on a server to create varieties of web applications. In this two day workshop the resource person introduced the basics of python programming language and students were made to execute simple tasks such as calculator, email ID creation etc. By using python Dr.Thirumaleshwara Bhat, Principal encouraged during the inauguration of the workshop, the students to learn new things and latest technologies. Dr.Sachin Bhat, HOD of ECE department appreciated the students and also highlighted upon the need to update one-self with the current technologies.

Dr. Ganesh Aithal, Vice-principal motivated the students and mentioned the significance of python programming in academics for career opportunities. Ms. Nisha D'souza, 3rd Year ECE student compered the program. Ms. Shashikala R coordinated the program. ECE faculty members were present during the inauguration of the workshop. The workshop has provided hands on training of python with GUI.

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SMVITM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

in association with

ISTE STUDENT CHAPTER &

KARUNADU TECHNOLOGIES PVT. LTD.

All are Cordially invited to the

Inaugural Function of

Two days hands-on workshop on

PYTHON & GUI

Chief Guest
Mahesh Deginal
Karunadu Technologies Pvt. Ltd.

Presided by
Prof. Dr. Thirumaleshwara Bhat
Principal, SMVITM

10 January 2023 at 9.15 AM
Venue: EC010, ECE Department

SMVITM - Engineering your Career and Character with Care

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10. Workshop on "ARDUINO APPLICATIONS"

The Institution Innovation Council and Indian Society for Technical Education of Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal in association with Atal Tinkering Lab, Karnataka Public School Hiriadka, Udupi organized a hands-on workshop on "ARDUINO APPLICATIONS" on 12th January 2023. Mr. Sandesh Kumar, Sr. Asst. Professor, ECE Dept.,along with students of SMVITM, Prasanna Shet, Ankitha Annappa Shet, Pratham, Rahul Manjunatha Poojari and Rimsha were the resource persons.

The students of SMVITM conducted a session on Arduino and its programming for around 55 students and they demonstrated various application circuits using Arduino kits. The students were divided into groups and were given an opportunity to do hands-on and learn how to program using Arduino kits.

11. Alumni Interaction on "Roadmap to Data Science & Analytical Industry"

Department of Electronics and Communication Engineering in association with ISTE Student Chapter and Alumni Cell had organized an Alumni Interaction Session on 21-04-2023 at 12:00p.m in EC011 (ECE Department). Mr. Bharath Shenoy, Human Resource Executive-System & Analytics, Intelliswift Software Inc. was the resource person.

At the beginning of session a short introduction to the topics of Data Science and Data Analytics were given with examples, which helped the students to relate the topics to the realtime applications. The comparison between the two fields facilitated to distinguish betweenthem. The roadmap to become a data scientist and the data analyst roadmap gave knowledge about the different fields of science and engineering that are required to become a successful data scientist and data analyst. Along with these, non-tech domain knowledge, data analytics learning and development tools available were also discussed. The variety of opportunities in the field of data science and data analytics was highlighted.

At the end, the importance of acquiring technical skills and knowledge along with current marketing trends were briefed. Ms. Ankitha Bhat, 6th semester, ECE was the Master of the Ceremony. Mr. Chetan R, Secretary/Treasurer ISTE as a concluding remark addressed the students about the importance of alumni interaction and current trends in the industry.

Dr. Guruprasad, In charge HoD, Department of Electronics and Communication

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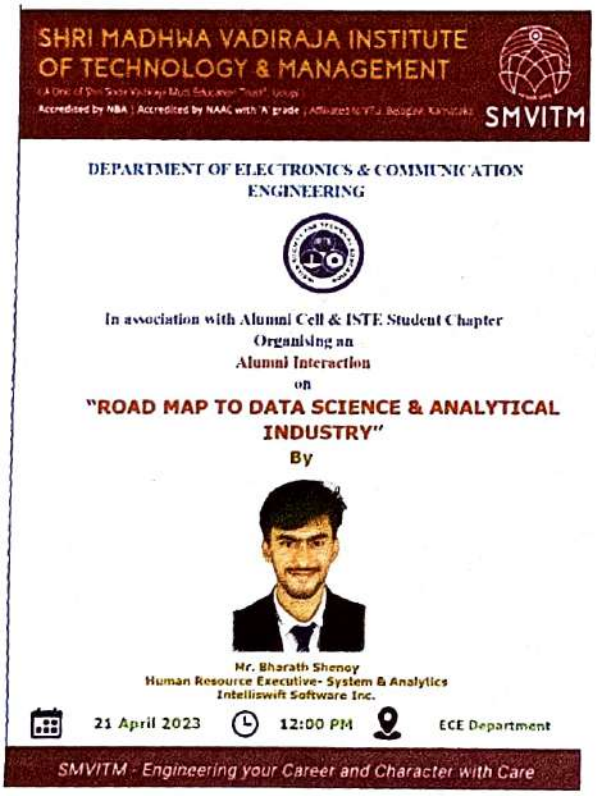
Engineering, and Ms. Chandana, ISTE Department Coordinator were present during the event. The event was coordinated by Ms. Chandana, ISTE Department Coordinator and Ms. Rajashree Nambiar, Alumni Cell coordinator with the support of Mr. Chetan R, Secretary/Treasurer ISTE.



12. Internship opportunities in LABVIEW by Mr. Satyanarayana

On 20 June, 2023, Mr. Satyanarayana from VI Solutions, Bengaluru, delivered a talk on internship opportunities in LabVIEW, AI, and ML. The talk aimed to highlight the significance of these technologies and the potential career prospects they offer for the current 6th semester students.

He further summarized that LabVIEW: LabVIEW is a graphical programming environment used in industries like manufacturing, research, and development. VI Solutions offers LabVIEW internships focusing on application development, user interface design, and data acquisition systems.

AI and ML: The speaker emphasized the importance of AI and ML across domains. VI Solutions also provides internships in AI and ML, covering model development, data analysis, and real-world applications.

The talk shed light on internship opportunities in LabVIEW, AI, and ML offered by VI Solutions. These internships bridge the gap between theory and practice, equipping participants with valuable skills and experience for future careers in these fields. Around 60 students attended the talk with Mr. Ranjith Bhat coordinating the event.

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ACCOMPLISHMENTS

13. Faculty Conference Publications

Sl.No.	Name of Authors	Title of paper	Name of conference
1	Ganesh shetty	The Classification of Satellite Galaxies Based on Convolution Neural Networks Machine Learning Algorithm	3rd International Conference for Emerging Technology (INCET 2022)
2	Arun Upadhyaya	A Security Enhanced Image Encryption and Compression Using Residue Number System and Discrete Cosine Transform	2nd International Conference on On Signal & Data Processing (ICSDP 2022)
3	Rajashree Nambiar	The Use of Privacy Preserving techniques in Edge Cloud Computing : A Study of Alternative approaches to Face Recognition	ICICICT-2022, Kannur India
4	Yogeshwary B. H	Leaf Disease Detection And Prevention Using Deep Learning	IEEE International Conference on Artificial Intelligence and Data Engineering (AIDE-2022)
5	Yogeshwary B. H	Iterative Localization technique for underwater wireless communication	IEEE NKCon-2022
6	Arun Upadhyaya	Significance of Performance Indicators (PI) in the Design of Course file-Case Study for Effective Teaching Pedagogy	24th ISTE Karnataka State Level Faculty Convention & 32nd Dr.L.S.Chandrakant Memorial Lecture Series
7	Ranjith Bhat	A comparative study on Alternative Deep Learning Based Animal Classification System	2nd Student International Conference [ICRDSTEM-2023]
8	Ranjith Bhat	Multiclass Classification Of Kidney Stone, Cyst, Tumor And Normal Using Deep Learning	JETRI-2023

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9	Chandana	A comparative study on Alternative Deep Learning Based Animal Classification System	2nd Student International Conference [ICRDSTEM-2023]
10	Guruprasad, Chetan R, Akshatha A R	Performance Analysis of Non-overlapping Two Phase Clock Signal Generators	12th IEEE International Conference on Communication Systems and Network Technologies
11	Shreya Udupa S, Sneha J S, Tulasi D J , MYashwanth Naik and Chetan R	Robot Assistance for Visually Impaired	"Technology for Industry 4.0 Revolution (ICTIR)"
12	Chandana	Brain Tumor Detection Using Deep Learning Techniques	IC-ICIC-2023
13	Rakshath Kumar, Akshay, Pratheeksha, Rashmitha Bhat, Chetan R, Dr. Guruprasad	Automatic Wireless Electricity Meter Reading System	"Technology for Industry 4.0 Revolution (ICTIR)"

14. Faculty Journal Publications

Sl.No.	Name of Authors	Title of paper	Name of Journal
1	Yogeshwary Bommenahalli Huchegowda; Aravind Bettadahalli Ningappa; Naveen Kumar C. M.; Yashwanth Nanjappa	Performance of SALP Swarm Localization Algorithm in Underwater Wireless Sensor Networks	Open Access Journal by MDPI
2	Yogeshwary B H	Performance of SALP Swarm Localization Algorithm in Underwater Wireless Sensor Networks	Photonics
3	Chaithra Kulal,	Detection of Pressure points on Diabetic	Journala of Emerging

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	Dheeraj,Meghana Bhat, Neema B Shetty, Nagaraja Rao	foot	Technologies aand Innovative Research (JETIR)
4	Shrava S, Shreya K, Shwetha Prabhu, Sinchana, Arun Upadhyaya	Image Encryption based on 3D Chaotic Map	IJARSE
5	Nagaraja Rao, Shantharama Rai C	Stability analysis and speed control of brushless DC motor based on self-ameliorate soft switching control methods	International Journal of Electrical and Computer Engineering (IJECE)

15.Faculty Development Programme & Workshops

Sl.No.	Name of Faculty	Title of the FDP or Workshop	Venue/College Name
1	Akshatha Rao L	UTKARSH	SMVITM
2	Akshatha Rao L	Joy of Computing using Python	NPTEL, Course, IITM
3	Akshatha Rao L	"Inculcating Universal Human Values in Technical Education"	AICTE
4	Arun Upadhyaya	Natural Language Processing	SMVITM, Bantakal
5	Arun Upadhyaya	UTKARSH	SMVITM
6	Arun Upadhyaya	Introduction to Python Programming and its applications	AICTE-VTU
7	Chandana	UTKARSH	SMVITM
8	Chandana	Inculcating Universal Human Values in Technical Education	AICTE
9	Chandana	Health care Analytics	SMVITM
10	Chandana	Artificial Intelligence and Machine Learning for Image Analysis - Matlab & Python Perspective	CMR Institute of Technology, Bengaluru
11	Chetan R	"Inculcating Universal Human Values in Technical Education"	AICTE
12	Chetan R	Introduction to Python Programming and its applications	AICTE-VTU
13	Ganesh Shetty	Natural Language Processing	SMVITM, Bantakal
14	Ganesh Shetty	Cryptography and network security	NPTEL, Course, IIT Madras

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15	Guruprasad	UTKARSH	SMVITM
16	Jayashree M	UTKARSH	SMVITM
17	Jayashree M	Five days Workshop on Signal Processing for Biomedical Applications	NMAMIT, Nitte
18	Jayashree M	Introduction to Python Programming and its applications	AICTE-VTU
19	Lahari Vaidya	UTKARSH	SMVITM
20	Nagaraja Rao	Natural Language Processing	SMVITM, Bantakal
21	Nagaraja Rao	Importance of Data Science in Machine Learning and its applications	RVITM,Bengaluru
22	Pavithra Poornima S	UTKARSH	SMVITM
23	Pavithra poornima S	"Inculcating Universal Human Values in Technical Education"	AICTE
24	Pavithra poornima S	Adithya-L1 Science and Education Outreach program	Pilikula Regional science centre, Mangaluru
25	Pavithra poornima S	Stay Safe online Compaign	Ministry of Electronics and Information Technology
26	Pavithra poornima S	Drones and Autonomous System organised by centre of Excellence Drones	CMRIT, Bengaluru
27	Pavithra poornima S	Idea Generation Method	ICT academy
28	Poojashree Hebbar	UTKARSH	SMVITM
29	Rajashree Nambiar	Machine Learning, Artificial Intelligence And Deep Learning Applications	NMAMIT, Nitte
30	Rajashree Nambiar	NLP Applications	SMVITM, Bantakal
31	Rajashree Nambiar	Artificial Intelligence and Machine Learning for Image Analysis - Matlab & Python Perspective organized	CMR Institute of Technology, Bengaluru
32	Ranjith Bhat	Machine Learning, Artificial Intelligence And Deep Learning Applications	NMAMIT, Nitte
33	Ranjith Bhat	NLP Applications	SMVITM, Bantakal
34	Ranjith Bhat	Artificial Intelligence and Machine Learning for Image Analysis - Matlab & Python Perspective organized	CMR Institute of Technology, Bengaluru
35	Sachin Prabhu K	UTKARSH	SMVITM
36	Sachin Prabhu K	"Inculcating Universal Human Values in Technical Education"	AICTE
37	Sachin Prabhu K	Introduction to Python Programming and its applications	AICTE-VTU
38	Sandesh Kumar	UTKARSH	SMVITM, Bantakal
39	Mr. Sandesh Kumar	"Inculcating Universal Human Values in Technical Education"	AICTE

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40	Mr. Sandesh Kumar	Introduction to Python Programming and its applications	AICTE-VTU
41	Shashikala R	Research and Publication Ethics	Nitte Meenakshi Institute of Tehnology
42	Shashikala R	Introduction to Python Programming and its applications	AICTE-VTU
43	Sowmya Bhat	Natural Language Processing	SMVITM, Bantakal
44	Yogeshwary B H	UTKARSH	SMVITM, Bantakal
45	Yogeshwary B H	Natural Language Processing	SMVITM, Bantakal
46	Yogeshwary B H	Introduction to Python Programming and its applications	AICTE-VTU
47	Vijayalatha Devadiga	UTKARSH	SMVITM
48	Vijayalatha Devadiga	Inverse Problems and Applications	NITK,Surathkal
49	Vijayalatha Devadiga	Introduction to Python Programming and its applications	AICTE-VTU
50	Vijayalatha Devadiga	Stay Safe online Compaign	Ministry of Electronics and Information Technology

16. KSCST/VGST Funded Project Details

➢ Start-up grant by Govt. of Karnataka

Dr. Sachin S Bhat, Head of the Department, Electronics and Communication Engineering of Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal had won the prestigious Karnataka State Urban Mobility Grand Challenge conducted by the Department of Electronics, IT, BT, Government of Karnataka. He won the startup grant of Rs. 10 lakhs for his work to assist the Police department in capturing the accident information on-site with minimal manual inputs and to register an online First Information Report. This tool uses Artificial Intelligence technique to extract information of accidents from photographs from an image captured at the accident spot and notifies the nearest hospital regarding the location and severity of accident. Principal and management have congratulated Dr. Sachin Bhat for his stupendous achievement.

➢ Start-Up funding from Government of India

Dr. Sachin Bhat, the Head of the E& C department of Shri Madhwa Vadiraja Institute of Technology and Management, Bantakal has received the funding assistance of Rs. 11.5 Lakh for his innovative idea titled "SURGICAL SPONGE DETECTION SYSTEM" under the MSME incubation scheme. Through the MSME scheme, a focus is placed on fostering emerging technologies and knowledge based innovative ventures that contribute to the global economy beyond the traditional activities of MSMEs.

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➢ Project funding from KSCST

Under the 45th series of Student Project Program (SPP), the evaluation committee had selected the projects submitted by SMVITM students for the sponsorship. Following are the sponsored project lists:

- Mr. Tejas S R, Mr. Subramanya S Nayak, Mr. Suraj S, Mr. Charan R Devadiga, Final year ECE students under the guidance of Ms. Sowmya Bhat had received the funding for the project titled "supplemental system for assisting the knee joint using pascal's law".
- Ms. Neha Kini, Ms. Nayak Dhanashree, Ashok, Ms. Shreya S Navelkar, Final year ECE students under the guidance of Mr. Chetan R had received the funding for the project titled "Embedded Based Automatic Lawn Mover".
- Mr. Rajesh C, Mr. Vikas N Rao, Ms. Riya Prabhu, Ms. Rakshitha R Nayak, Final year ECE students under the guidance of Dr.Balachandra Achar had received the funding for the project titled "Agricultural Drone".
- Mr. Karthik N, Ms. Hrishika, Mr. Arun J K, Final year ECE students under the guidance of Ms. Akshatha Rao had received the funding for the project titled "Design And Development Of Negative Pressure Wound Therapy Device".
- Ms. Shreya Udupa S, Ms. Sneha J S, Ms. Tulasi D J and Mr. Yashwanth Naik, Final year ECE students under the guidance of Mr. Chetan R had received the funding for the project titled "Robot Assistance for the Visually Impaired".

17.PLACEMENTS

Placed Student Details in the Interval of June 2022-January 2023		
S.I.	**Student Name**	**Company name**
1	Akshatha Anil Kumar Renjal	Tech Mahindra - Cerium Systems (P) Ltd
2	Hrishika	Tech Mahindra - Cerium Systems (P) Ltd
3	Srinidhi S K	Tech Mahindra - Cerium Systems (P) Ltd
4	Adithi Girish	Kyndryl India Pvt. Ltd., Bengaluru
5	Rachana	Kyndryl India Pvt. Ltd.
6	Sameeksha P U	Kyndryl India Pvt. Ltd.
7	Shanthika	Kyndryl India Pvt. Ltd.
8	Shreya Udupa S	Kyndryl India Pvt. Ltd.
9	Lohith V P	Trianz
10	Bhoomika	SKOLAR
11	Prajwal Upadhya	Hexaware Technologies Ltd.
12	Prasanna Nayak	Robosoft Technologies Pvt. Ltd., Udupi
13	Adithi P	SKOLAR Bengaluru
14	Akshay K G	SKOLAR Bengaluru
15	Anwitha Rao P	SKOLAR Bengaluru
16	Arun J Kundgolkar	SKOLAR Bengaluru
17	Dheeksha A Suvarna	SKOLAR Bengaluru
18	Harshitha Shetty	SKOLAR Bengaluru
19	Keerthan	SKOLAR Bengaluru
20	Prasthuthi Amin	SKOLAR Bengaluru
21	Rithesh Kumar	SKOLAR Bengaluru

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22	Sakshi	SKOLAR Bengaluru
23	Shanthkumar C K	SKOLAR Bengaluru
24	Sharanya (Santosh)	SKOLAR Bengaluru
25	Shreya	SKOLAR Bengaluru
26	Sukhitha Ks	Usha Armour Pvt. Ltd., Bengaluru
27	Sneha J S	iWave Systems Technologies Pvt. Ltd.,
28	Pratheeksha	Kambala Solutions Pvt. Ltd., Mangaluru
29	Varshini Acharya	Kambala Solutions Pvt. Ltd., Mangaluru
30	Sudeep	Lekha Wireless Solutions Pvt. Ltd
31	Varalakshmi	Lekha Wireless Solutions Pvt. Ltd
32	Chaithra Kulal	Rinex Technologies Pvt. Ltd., Bengaluru / Mangalore.
33	Karthik N	Rinex Technologies Pvt. Ltd., Bengaluru / Mangalore.
34	Meghana R Bhat	Rinex Technologies Pvt. Ltd., Bengaluru / Mangalore.
35	Neema B Shetty	Rinex Technologies Pvt. Ltd., Bengaluru / Mangalore.
36	Nishanth	TCS Ninja
37	Shwetha Prabhu	TCS Ninja
38	Prajwal	Tekworks Enterprise solutions pvt ltd
39	Dileep A R	Lekha Wireless Solutions Pvt. Ltd.
40	Rashmitha Bhat	Lekha Wireless Solutions Pvt. Ltd.
41	Shreya Upendra Nayak	Lekha Wireless Solutions Pvt. Ltd.
42	Hemanth V Prabhu	GlowTouch Technologies, Mangaluru
43	K Rakesh	Mirafra Software Technologies Pvt. Ltd.
44	Karthik N	Mirafra Software Technologies Pvt. Ltd.
45	Nikitha	Mirafra Software Technologies Pvt. Ltd.
46	Soujanya S	Mirafra Software Technologies Pvt. Ltd.
47	Swathi Bhat	Mirafra Software Technologies Pvt. Ltd.
48	Sumukha Hatwar K N	Tantragyaan Solutions, Bangalore
49	Chandrakala	Vintrus EduTech, Bengaluru
50	Kirana D N	Vintrus EduTech, Bengaluru
51	Rithesh Kumar	Manipal Technologies Limited, Manipal
52	Ujwal U Shetty	Seventh Sense Talent Solutions, Bengaluru
53	Dheeraj	Karmic Design Private Limited, Manipal
54	Divyashree	Karmic Design Private Limited, Manipal
55	Rakshath Kumar	Karmic Design Private Limited, Manipal

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18. Internship Details

Sl No.	USN	NAME OF THE STUDENT	NAME OF THE COMPANY/ ORGANISATION	PLACE	START DATE	END DATE
1	4MW19EC001	ADITHI GIRISH	SMVITM	BANTAKAL	22/08/2022	22/09/2022
2	4MW19EC002	ADITHI P	NMAMIT	NITTE	22/08/2022	22/09/2022
3	4MW19EC003	ADITHYA S BHAT	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
4	4MW19EC004	AKSHATHA ANILKUMAR RENJAL	SMVITM	BANTAKAL	22/08/2022	22/09/2022
5	4MW19EC005	AKSHAY	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
6	4MW19EC006	AKSHAY K G	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
7	4MW19EC007	ANWITHA RAO P	NMAMIT	NITTE	22/08/2022	22/09/2022
8	4MW19EC008	ARUN J KUNDGOLKAR	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
9	4MW19EC009	BHOOMIKA	NEXTEER	BENGALURU	23/08/2022	23/09/2022
10	4MW19EC010	CHAITHRA KULAL	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
11	4MW19EC011	CHANDRAKALA	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
12	4MW19EC012	CHAYA NAIK	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
13	4MW19EC013	DEEPA NAYAK	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
14	4MW19EC014	DHEEKSHA A SUVARNA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
15	4MW19EC015	DHEERAJ	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
16	4MW19EC016	DILEEP A R	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
17	4MW19EC017	DIVYASHREE	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
18	4MW19EC018	HARSHITHA SHETTY	NMAMIT	NITTE	22/08/2022	22/09/2022
19	4MW19EC019	HEMANTH V PRABHU	SMVITM	BANTAKAL	22/08/2022	22/09/2022
20	4MW19EC020	HRISHIKA	INVENTERON TECHNOLOGIES	BENGALURU	25/08/2022	24/09/2022
21	4MW19EC021	K RAKESH	SMVITM	BANTAKAL	22/08/2022	22/09/2022
22	4MW19EC022	K SRINIVAS KAMATH	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
23	4MW19EC023	KARTHIK N	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
24	4MW19EC024	KEERTHAN	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
25	4MW19EC025	KIRANA D N	SMVITM	BANTAKAL	22/08/2022	22/09/2022
26	4MW19EC026	LOHITH V P	SMVITM	BANTAKAL	22/08/2022	22/09/2022
27	4MW19EC027	MANTHANA K	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
28	4MW19EC028	MEGHANA BAPAT K	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
29	4MW19EC029	MEGHANA R BHAT	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
30	4MW19EC030	MENAKA R J	RADIO STATION	MANGALURU	22/08/2022	17/09/2022
31	4MW19EC031	NEEMA B SHETTY	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
32	4MW19EC032	NIKITHA	RADIO STATION	MANGALURU	22/08/2022	17/09/2022

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33	4MW19EC033	NISHANTH	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
34	4MW19EC034	PRAJWAL	SMVITM	BANTAKAL	22/08/2022	22/09/2022
35	4MW19EC035	PRAJWAL UPADHYA	SMVITM	BANTAKAL	22/08/2022	22/09/2022
36	4MW19EC036	PRASANNA NAYAK	SMVITM	BANTAKAL	22/08/2022	22/09/2022
37	4MW19EC037	PRASTHUTHI AMIN	RADIO STATION	MANGALURU	22/08/2022	17/09/2022
38	4MW19EC038	PRATHEEKSHA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
39	4MW19EC040	RACHANA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
40	4MW19EC041	RAKSHATH KUMAR	TECH FORTUNE TECHNOLOGIES	HUBBALLI	25/08/2022	25/09/2022
41	4MW19EC043	RAKSHITHA R NAYAK	INVENTERON TECHNOLOGIES	BENGALURU	25/08/2022	24/09/2022
42	4MW19EC044	RASHMITHA BHAT	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
43	4MW19EC045	RITHESH KUMAR	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
44	4MW19EC046	RUHAIMA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
45	4MW19EC047	SAKSHI	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
46	4MW19EC048	SAMEEKSHA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
47	4MW19EC049	SAMEEKSHA P U	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
48	4MW19EC050	SHANTHIKA	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
49	4MW19EC051	SHANTHKUMAR C K	SMVITM	BANTAKAL	22/08/2022	22/09/2022
50	4MW19EC052	SHARANYA (U UDAYA)	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
51	4MW19EC053	SHARANYA (SANTOSH)	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
52	4MW19EC054	SHETTY NITHIN VIJAY	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
53	4MW19EC055	SHRAVAN S	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
54	4MW19EC056	SHREEPATHI	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
55	4MW19EC057	SHREESHA S AITHAL	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
56	4MW19EC058	SHREESHA	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
57	4MW19EC059	SHREYA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
58	4MW19EC060	SHREYA DEVADIGA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
59	4MW19EC061	SHREYA UDUPA S	NMAMIT	NITTE	22/08/2022	22/09/2022
60	4MW19EC062	SHREYA UPENDRA NAYAK	BHARATH ELECTRONICS LIMITED	ANDHRA PRADESH	22/08/2022	22/09/2022
61	4MW19EC063	SHREYAS ACHARYA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
62	4MW19EC064	SHREYAS M NAIK	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
63	4MW19EC065	SHRIKRISHNA BHAT	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
64	4MW19EC066	SHRINIKETH	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
65	4MW19EC068	SHWETHA	SWAGEN	BENGALURU	29/08/2022	30/09/2022

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		PRABHU				
66	4MW19EC069	SIJAL KUMARI	WEBDEV IT SOLUTIONS	BIHAR	25/08/2022	25/09/2022
67	4MW19EC070	SINCHANA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
68	4MW19EC071	SNEHA J S	KYUNGSHIN INDUSTRIAL MOTHERSON PRIVATE LIMITED	TAMIL NADU	29/08/2022	29/09/2022
69	4MW19EC072	SOUJANYA S	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
70	4MW19EC074	SRIJANYA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
71	4MW19EC075	SRINIDHI S K	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
72	4MW19EC076	SUDEEP	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
73	4MW19EC077	SUKHITHA K S	BHARATH ELECTRONICS LIMITED	ANDHRA PRADESH	22/08/2022	22/09/2022
74	4MW19EC079	SUMUKHA HATWAR K N	SMVITM	BANTAKAL	22/08/2022	22/09/2022
75	4MW19EC080	SWATHI BHAT	MESCOM	MANGALURU	25/08/2022	25/09/2022
76	4MW19EC081	TABISH AKBAR	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
77	4MW19EC082	TULASI D J	NMAMIT	NITTE	22/08/2022	22/09/2022
78	4MW19EC083	UJWAL U SHETTY	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
79	4MW19EC084	VARALAKSHMI	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
80	4MW19EC085	VARSHINI ACHARYA	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022
81	4MW19EC086	WILSON NORONHA	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
82	4MW19EC087	YASHASWINI R AMIN	NEXTEER	BENGALURU	22/08/2022	22/09/2022
83	4MW19EC088	YASHWANTH NAIK	LOGIN WARE	BENGALURU	25/8/2022	25/09/2022
84	4MW20EC400	SUJAN	VI SOLUTIONS	BENGALURU	01-08-2022	20/08/2022

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19. PROJECT AWARDS

Co-curricular committee in association with ISTE student chapter and IIC of SMVITM, conducted Final Year Project Exhibition on account of National Technology Day in the institute premises. Experts nominated a total of 2 student projects as Best Projects from each department. The I prize was 3,000 and II prize was 2,000 cash was awarded at a farewell function on 13th May2023. Program was coordinated by cocurricular co-ordinator Dr. Renita Sharon Monis.

The project titled **"DRY AND WET GARBAGE SEGREGATION & MONITORING"**, has won the best project award under the exhibition category and this project was completed by the final year students **Sudeep, Ujwal U Shetty, Wilson Noronha & Sujan** from Electronics and Communication Engineering department under the guidance of Ms. Vimitha, Asst. Professor, ECE Dept.

The project titled **"AUTOMATIC ENERGY METER READER"**, has won the runner up under the exhibition category and this project was completed by the final year students **Akshay, Pratheeksha, Rakshath Kumar & Rashmitha Bhat** from Electronics and Communication Engineering department under the guidance of Dr. Guruprasad, Associate Professor, ECE Dept.

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20. MINI PROJECT EXHIBITION & COMPETITION AWARDS

Co-curricular committee in association with ISTE student chapter of SMVITM and Hobby Project Club, conducted Mini Project Exhibition in the institute premises. Experts nominated a total of 3 student projects as Best Projects and three projects as consolation Prizes. The I prize was 3,000 and II prize was 2,000 cash and III prize was 1,000 .

The Mini project titled **"IOT BASED SMART CLASSROOM AND HOME AUTOMATION"**, has won the best mini project award and this mini project was completed by the pre final year students **Prasanna Shet, Pratham, Ankitha Shet, Rahul** from Electronics and Communication Engineering department under the guidance of Mr. Sachin Prabhu, Sr. Asst. Professor, ECE Dept.

The mini project titled **"ECO-TECH"**, has won the runner up and this mini project was completed by the second year students **Akshata Muralidhara Bailoor, & Dhanush Devadas Shasthri** from Electronics and Communication Engineering department under the guidance of Mr. Nagaraj Rao Associate Professor, ECE Dept.

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TOPPERS LIST WITH SGPA

8TH SEMESTER

1	4MW19EC034	PRAJWAL	9.44
2	4MW19EC050	SHANTHIKA	9.44
3	4MW19EC004	AKSHATHA ANILKUMAR RENJAL	9.33

6TH SEMESTER

1	4MW20EC024	KEERTHANA	9.08
2	4MW20EC012	ANUSHA	9.04
3	4MW20EC035	NIKHITHA SHETTY	8.83

3RD SEMESTER

1	4MW21EC013	CHAITANYA ANANT NILEKANI	9.39
2	4MW21EC073	U ASHLESH KUMAR	9.22
3	4MW21EC027	KEERTHANA K	9.17

FACULTIES ACHEIVEMENTS

Dr. Guruprasad

- Reviewed papers in the stream "Embeded system and IOT" for the conference organized by the department of Electronics and Communication Engineering, NMAMIT, Nitte during 22 and 23 December 2022.

Mr. Nagaraja Rao

- Participated in IP Awareness/Training program under National Intellectual Property Awareness Mission on August 03,2022 organized by intellectual property office india
- Reviewed papers in the stream "Embedded Systems & IOT" for the International conference on VLSI, SIGNAL PROCESSING, POWER ELECTRONICS, IOT, COMMUNICATION AND EMBEDDED SYSTEMS organized by the department of ECE, NMAM Institute of Technology, Nitte during 22 & 23 December 2022

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Mr. Arun Upadhyaya

- Invited speaker and delivering a Session on "Activity based learning on 28 September 2022 in a Faculty Development Program "Utkarsh" held at SMVITM College premises, Bantakal on 28, 30 September and 6 -8 October 2022.
- Reviewed papers for the VPSICE2022
- Resource person of "Value added course on Entrepreneurship" organized by the Institution's Innovation Council in association with the Entrepreneurship Development Cell on 20 June 2023.

Mr. Chetan R

- Judge for interhouse "Science in everyday life" exhibition held on 20/10/22.
- Support rendered in mentoring the students of SVH Highschool Innanje in the spirit of Anveshana 2023, Hubli-Dharwad
- Judge for the 24 hours state level hackathon competition " HACKOTHSAVA 2023 " organized by the Department of Computer Science and Engineering in association with the Institution's Innovation Cell and Indian Society for Technical Education held on 2 & 3 June 2023 at the college premises.
- Resource person for One day workshop on "Electric VLSI Design Systems" organised by the department of ECE, Institute of engineering and technology, Srinivasa University Mukka Mangaluru, under NICSA on April 13, 2023

Mr. Ganesh Shetty

- Completed the course cryptography and network security with a consolidated score of 83%

Mr. Ranjith Bhat

- Filed patent on INTELLIGENT LEARNING-BASED PREDICTION OF DATA CENTER LOAD EFFICIENCY IN CLOUD COMPUTING. Date of filing of Application :12/05/2022

Ms. Yogeshwary B.H

- Reviewed papers in International conference on technology engineering management for societal impact using marketing , entrepreneurship, and talent (TEMSMET 2023)", organized by the Vidya Vikas institute of technology Mysuru on 10th & 11th February 2023.

Ms. Akshatha Rao L

- Completed the course " The Joy of computing using python" with a consolidated score of 90%

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OUT GOING BATCH 2022-23

ECE BATCH 2022-23 (Section –A)

ECE BATCH-2022-23 (Section –B)

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CONGRATULATIONS

Ms. AKSHATHA ANILKUMAR RENJAL

GOLD MEDALIST OF ECE 2022-23 BATCH

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SMVITM

Department of
Electronics and Communication Engineering

Newsletter Editors:

Ms. Jayashree M, Asst. Professor

Mr. Chetan R, Sr. Asst. Professor

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Principal
SHRI MADHWA VADIRAJA
INSTITUTE OF TECHNOLOGY & MANAGEMENT
Vishwothama Nagar, Udupi Dist.
BANTAKAL - 574 115