Publications List

For Journal:
1. **Sowmya Bhat**,Kusuma Prabhu, Aruna M.S, Avinash N.J (June 2016), Design of ARM7 Processor Core With Constraint of Power and Area Consumption Using FSM Modeling and Random Logic Method, International Journal of Informative & Futuristic Research, Volume 3, Issue 10, page no. 3705-3717.
2. Avinash N.J,**Sowmya Bhat,** (August 2016), A Novel Approach of GSM Based Eco-Friendly Low Energy Consumption Smart Train With Enhanced Features, International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering Volume 4, Issue 8, page no. 104-106.
3. Kusuma Prabhu, **Sowmya Bhat**, Aruna M.S (June 2016),Secured Health Information Transmission,International Journal of Engineering Research in Electronic and Communication Engineering(IJERECE), Volume 3, Issue 6, page no.186-190.
4. **Sowmya Bhat**, Avinash N.J, Kusuma Prabhu, Rajashree Nambiar (September 2016),Design of Area Efficient Binary to Gray Code Converter Using Mentor Graphics,International Journal of Advanced Computing and Electronics Technology(IJACET), Volume 3, Issue 5, 12th September 2016.

For Conference:
1. **Sowmya Bhat,** Avinash N.J, Kusuma Prabhu, Rajashree Nambiar, (2016), Design of Area Efficient Binary to Gray Code Converter Using Mentor Graphics, 22nd International Conference on Electrical Electronics Communication Robotics and Instrumentation Engineering (ICEECIE 2016), Mysore, 11th September,2016, page no. from-to (if it is published in the conference proceedings).
2. Kusuma Prabhu, **Sowmya Bhat**, Aruna M.S, (2016), Secured Health Information Transmission, International Conference on Applied Science Engineering and Technology, Sri Sairam College of Engineering, Anekal- Bengaluru, 6th -7th June,2016, page no. from-to (if it is published in the conference proceedings).
3. **Sowmya Bhat**, (2014), Design of Low Power and Area Efficient Processor Core, National Conference on Emerging Trends in Communication and Biomedical Engineering (NCECB-2014),Sri Siddhartha Institute of Technology, Maralur, Tumkur,9th & 10th May,2014,
4. **Sowmya Bhat**, Taranath H.B, (2014) Design of Low Power and Area Efficient Soft Core Processor Using MATLAB Simulink, National Conference on Communication and Image Processing-NCCIP-14, T.John Institute of Technology, Bengaluru, 9th May,2014